Features

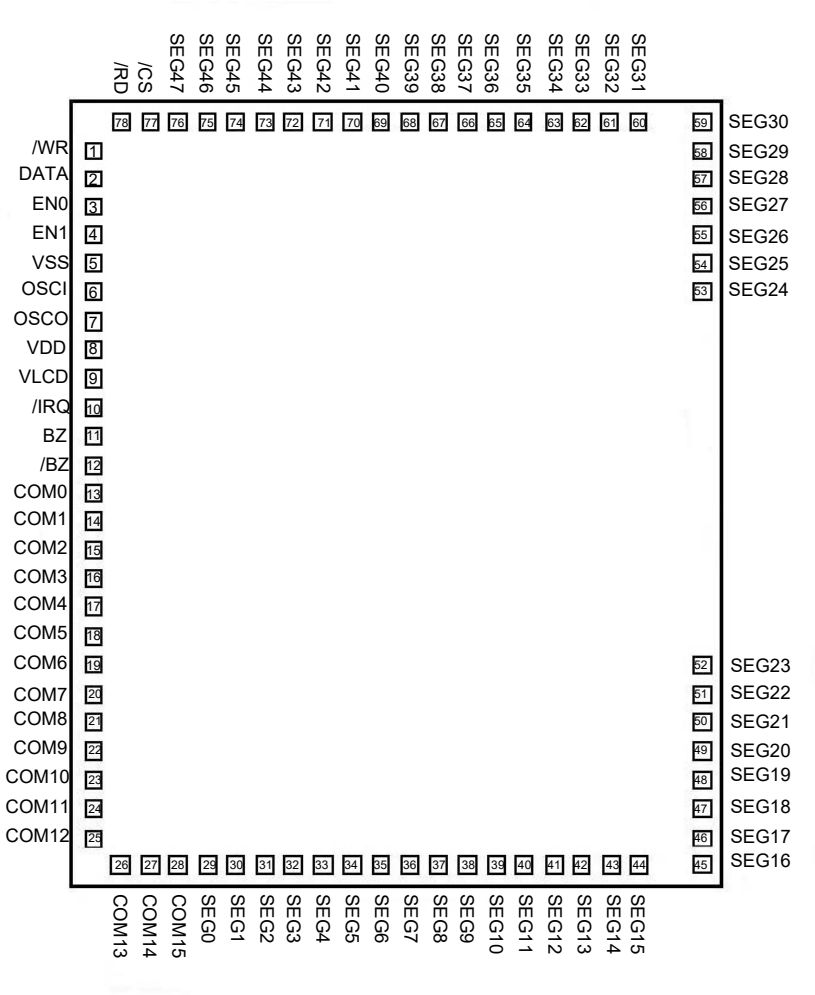
- Operating voltage:2.4-5.2V
- Built-in 32kHz RC oscillator（default）
- External 32kHz requency source
- 1/5 BIAS
- 1/16 duty (16 COM)
- Built-in 48×16 bit display RAM
- Selection of buzzer frequencies 2kHz、4kHz
- STANDBY mode（by Cmd LCD OFF,SYS DIS）
- 8 kinds of time base/WDT clock sources
- Time base or WDT overflow output （/IRQ pin）
- 3 or 4 wire serial interface
- Software configuration LCD parameters
- Data mode and command mode instructions
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage（≤VDD）
- Package:
  LQFP100(14.0mm x 14.0mm PP=0.5mm)
  QFP100(20.0mm x 14.0mm PP=0.65mm)
  DICE
  COG

1 General Description

VK1626 is a RAM Mapping 48x16 LCD Driver，It can support LCD screens with a maximum of 768 pattern(48SEGx16COM).Only 3 or 4 lines are required to communication interface with the VK1626,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command（by Cmd LCD OFF,SYS DIS）.

2 COB PAD description and Coordinates

2.1 COB PAD Assignment



Substrate: connected to VDD

PAD size: 90×90 um PAD spacing: 112 um

note: VLCD<VDD

2.2 COB PAD Coordinates

coordinate origin is in the center of the chip， unit：μm

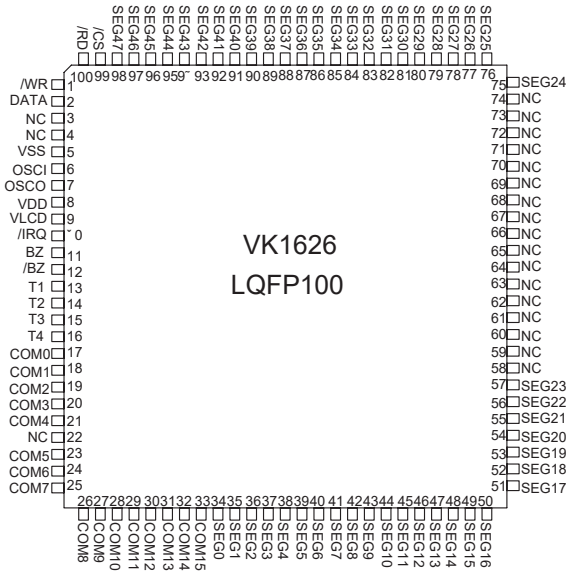
Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	/WR	75.8	3210	40	SEG11	1961.15	74.65
2	DATA	75.8	3085	41	SEG12	2086.15	74.65
3	EN0	75.8	2960	42	SEG13	2211.15	74.65
4	EN1	75.8	2835	43	SEG14	2336.15	74.65
5	VSS	75.8	2710	44	SEG15	2461.15	74.65
6	VSCI	75.8	2585	45	SEG16	2694.2	74.65
7	OSCO	75.8	2460	46	SEG17	2694.2	199.65
8	VDD	75.8	2335	47	SEG18	2694.2	324.65
9	VLCD	75.8	2210	48	SEG19	2694.2	449.65
10	/IRQ	75.8	2085	49	SEG20	2694.2	574.65
11	BZ	75.8	1960	50	SEG21	2694.2	699.65
12	/BZ	75.8	1835	51	SEG22	2694.2	824.65
13	COM0	75.8	1710	52	SEG23	2694.2	949.64
14	COM1	75.8	1585	53	SEG24	2694.2	2595.35
15	COM2	75.8	1460	54	SEG25	2694.2	2720.35
16	COM3	75.8	1335	55	SEG26	2694.2	2845.35
17	COM4	75.8	1210	56	SEG27	2694.2	2970.35
18	COM5	75.8	1085	57	SEG28	2694.2	3095.35
19	COM6	75.8	960	58	SEG29	2694.2	3220.35
20	COM7	75.8	835	59	SEG30	2694.2	3345.35
21	COM8	75.8	710	60	SEG31	2461.15	3345.35
22	COM9	75.8	585	61	SEG32	2336.15	3345.35
23	COM10	75.8	460	62	SEG33	2211.15	3345.35
24	COM11	75.8	335	63	SEG34	2086.15	3345.35
25	COM12	75.8	210	64	SEG35	1961.15	3345.35
26	COM13	211.15	74.65	65	SEG36	1835.15	3345.35
27	COM14	336.15	74.65	66	SEG37	1711.15	3345.35

coordinate origin is in the center of the chip， unit：μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y
28	COM15	461.15	74.65	67	SEG38	1586.15	3345.35
29	SEG0	586.15	74.65	68	SEG39	1461.15	3345.35
30	SEG1	711.15	74.65	69	SEG40	1336.16	3345.35
31	SEG2	836.15	74.65	70	SEG41	1211.15	3345.35
32	SEG3	961.15	74.65	71	SEG42	1086.15	3345.35
33	SEG4	1086.15	74.65	72	SEG43	961.15	3345.35
34	SEG5	1211.15	74.65	73	SEG44	836.15	3345.35
35	SEG6	1336.15	74.65	74	SEG45	711.15	3345.35
36	SEG7	1461.15	74.65	75	SEG46	568.15	3345.35
37	SEG8	1586.15	74.65	76	SEG47	461.15	3345.35
38	SEG9	1711.15	74.65	77	/CS	336.15	3345.35
39	SEG10	1836.15.	74.65	78	/RD	211.15	3345.35

3 Pinouts and pin description

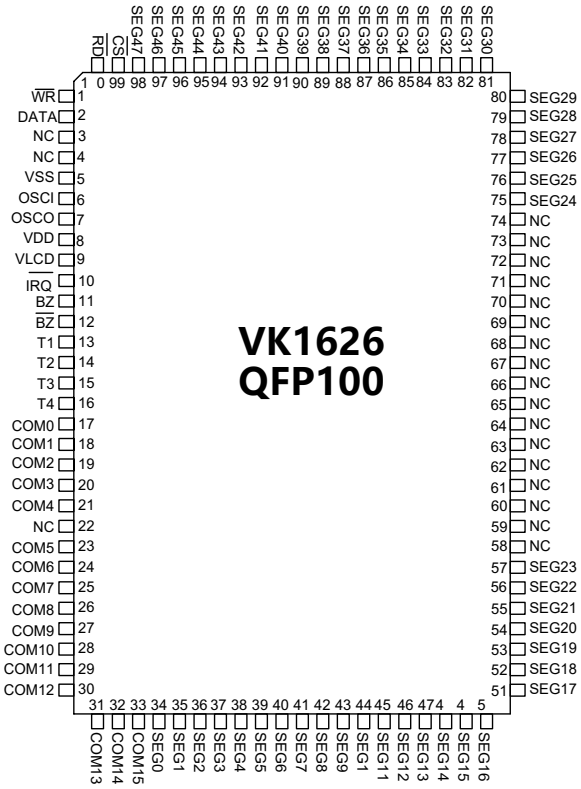
3.1 VK1626 LQFP100 Pin Assignment



3.2 VK1626 LQFP100 Pin Description

No.	Name	I/O	Function
99	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
100	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
1	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
2	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to an external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD power input
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-16	T1-T4	—	——
17-21 23-33	COM0-COM15	O	LCD COM outputs
34-57 75-98	SEG0-SEG47	O	LCD SEG outputs

3.3 VK1626 QFP100 Pin Assignment

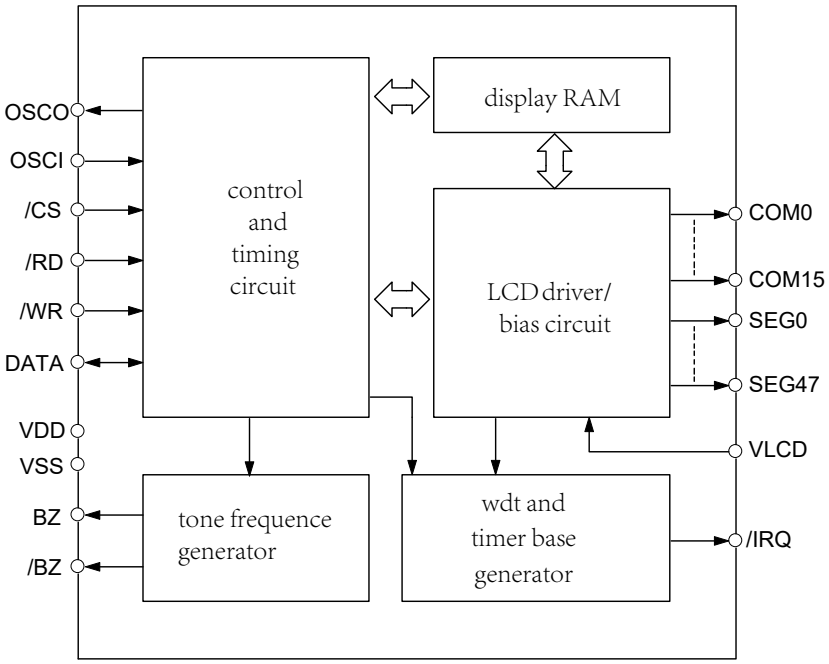


3.4 VK1626 QFP100 Pin Description

No.	Name	I/O	Function
99	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
100	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
1	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
2	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to an external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD power input
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-16	T1-T4	—	——
17-21 23-33	COM0-COM15	O	LCD COM outputs
34-57 75-98	SEG0-SEG47	O	LCD SEG outputs

4 Functional Description

4.1 Block diagram



4.2 Display RAM

The static display memory (RAM) is organized into 48×16 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands.

The following is a mapping from the RAM to the LCD pattern:

	COM15	COM14	COM13	COM12	---- ----		COM3	COM2	COM1	COM0		
SEG0					3						0	
SEG1					7						4	
SEG2					11						8	
SEG3					15	----					12	address 8 bits
⋮					⋮						⋮	（A7----A0）
SEG47					191						188	
	D3	D2	D1	D0	Data\Addr		D3	D2	D1	D0	Data\Addr	

4 bits data
（D3,D2,D1,D0）

4.3 Time Base and WDT

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT) is composed of an 8-stage time base generator along with a 2-stage count-up counter,it is designed to break the host controller from abnormal states such as unknown or unwanted jump, execution errors, etc.The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the /IRQ pin by a command option. There are totally 8 frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

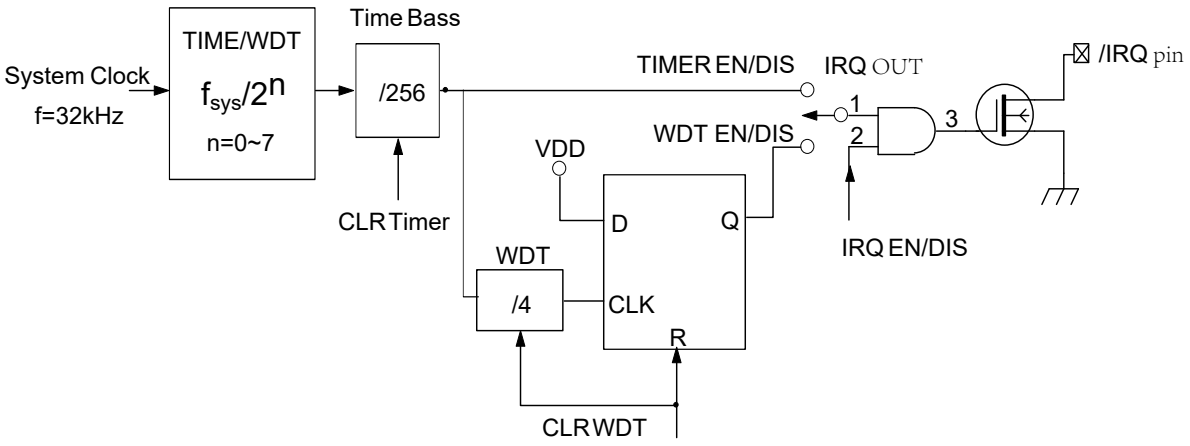
$$f_{WDT}=f_{sys}/2^{n} \quad (n=0\sim7) \qquad fsys=32kHz$$

The time base generator and WDT share the same 8-stage counter.WDT is cleared by executing the CLR WDT command,time base generator is cleared by executing the CLR WDT or the CLR TIMER command.

Executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the /IRQ pin). invoking the WDT DIS command disables the time base generator.After the TIMER EN command is transferred, the WDT is disconnected from the /IRQ pin, and the output of the time base generator is connected to the /IRQ pin.

The /IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command. After the system power on, the /IRQ will be disabled.

Timer and WDT Configurations:



4.4 Tone Output

VK1626 has a simple 2KHz / 4kHz tone generator， it can output a pair of differential driving signals on the BZ and /BZ, which are used to generate a single tone .By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable .The tone output can be turned on or off by invoking the TONE 4k/TONE 2k or the TONE OFF command. The tone outputs, namely BZ and /BZ, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the /BZ outputs will remain at low level.

4.5 LCD Driver

The VK1626 is a 768(48×16) pattern LCD driver, 1/5bias and 1/16duty (8 com).

4.5.1 Communication Interfacing

Four lines are required to interface with the VK1626.If only used for display, only 3 pins can be used.

The /CS pin is used to initialize the serial interface circuit and to terminate the communication with HOST.

The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The /RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the /RD signal, and the clocked out data will then appear on the DATA line.

The /WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into theVK1626 on the rising edge of the WR signal.

The /IRQ pin can be selected as a timer output or a WDT overflow flag output by the software setting,it is a NMOS open drain output.

4.5.2 Command Format

VK1626 can be configured by the Software setting. There are two mode commands to configure the LCD parameters and to transfer the LCD display data,The configuration mode of the VK1626 is called command mode, and its command mode ID is 1 0 0. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode IDs and the command mode ID:

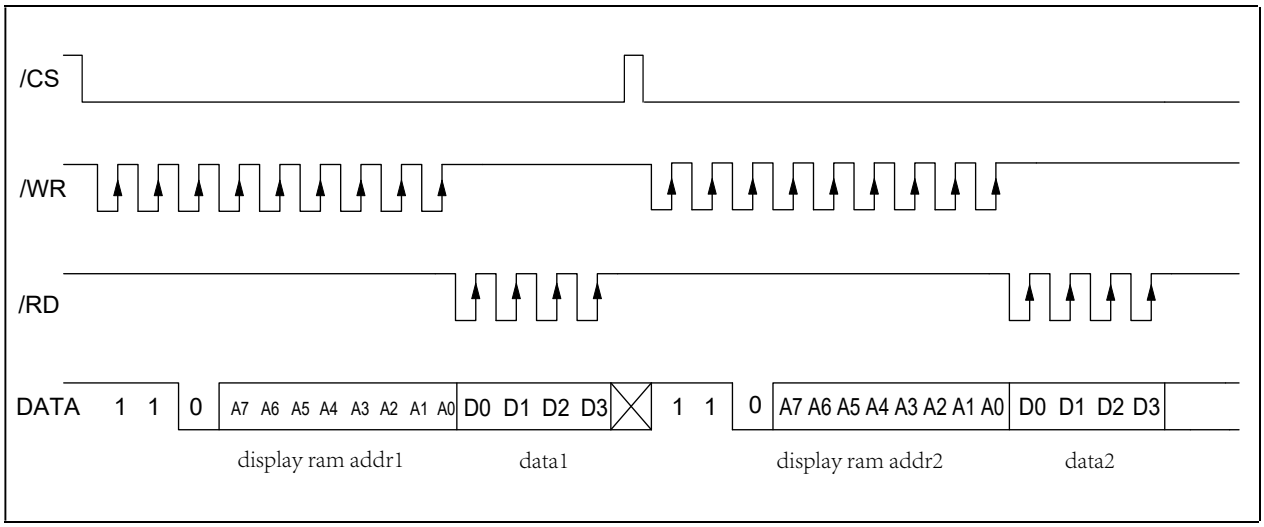
操作	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

4.5.3 Cmd/Data Timing Diagrams

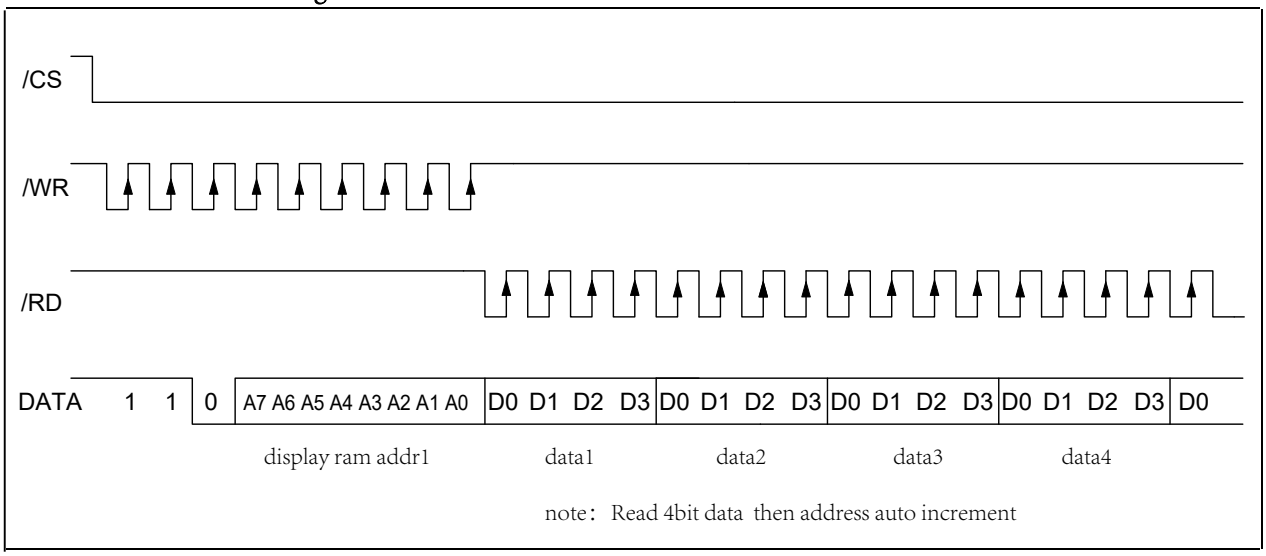
The following are the data mode IDs and the command mode ID Timing Diagrams。

4.5.3.1 READ Mode

Command Code : 110

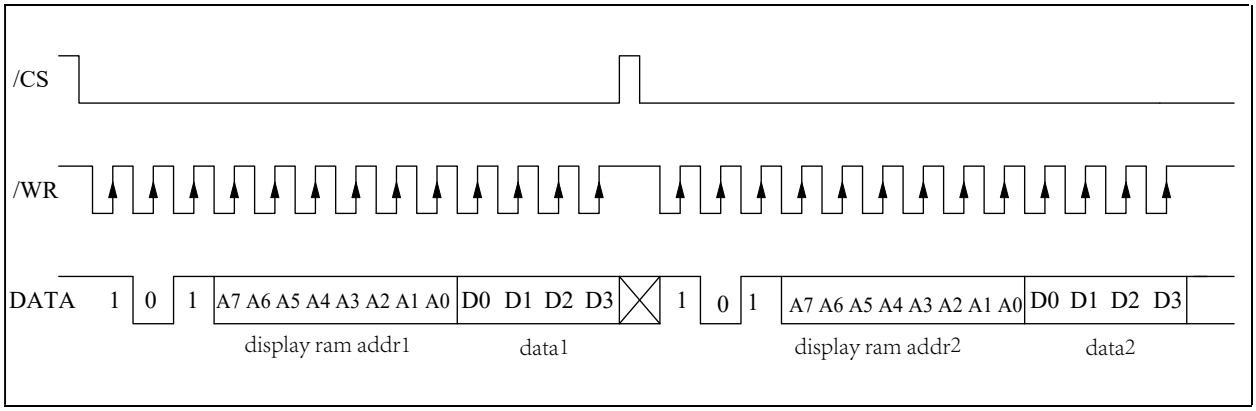


Successive Address Reading

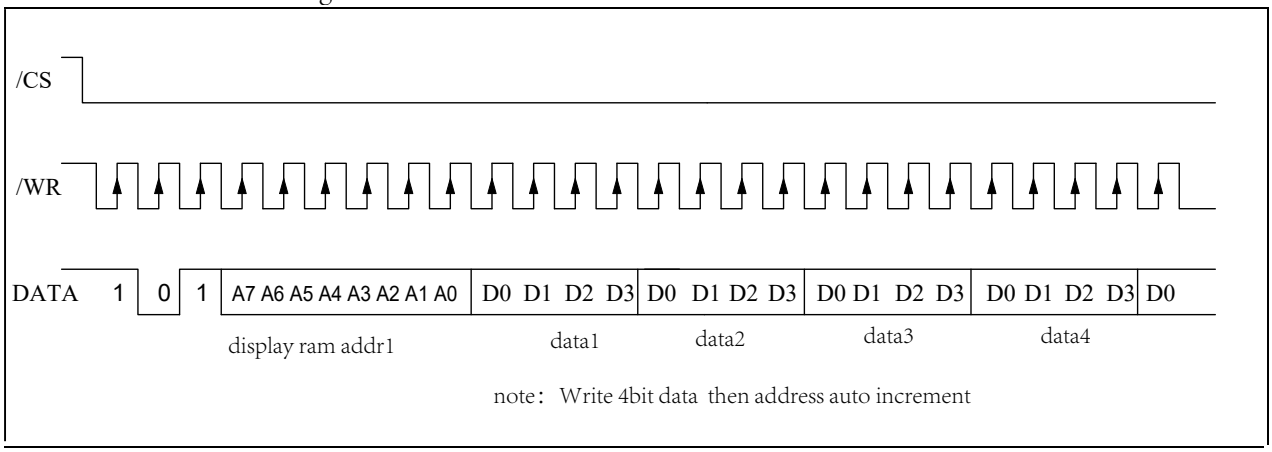


4.5.3.2 WRITE Mode

Command Code : 101

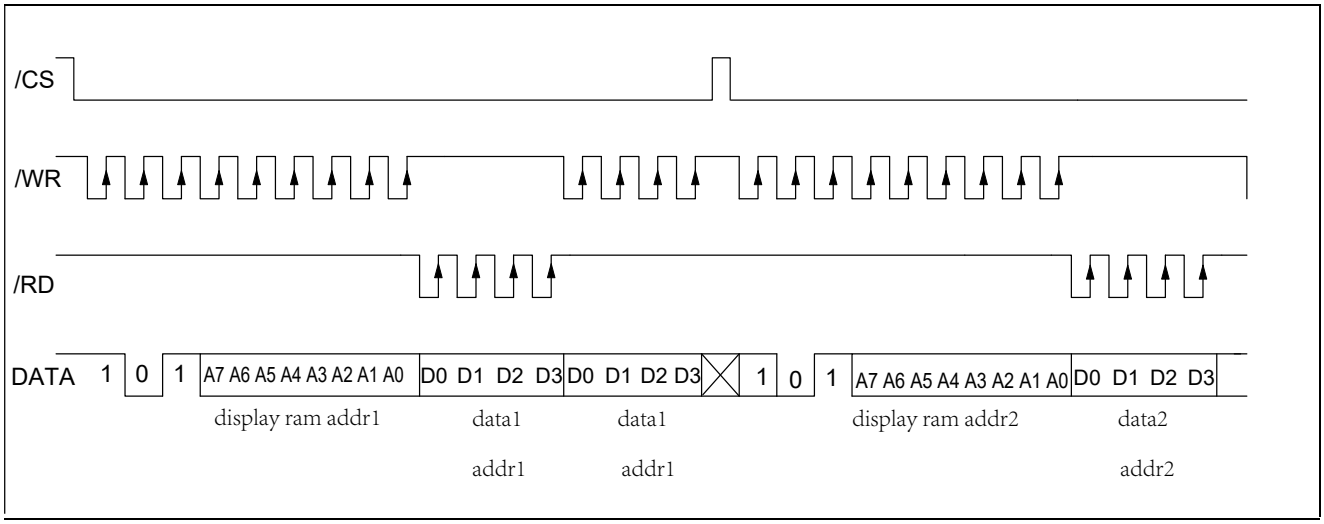


Successive Address Writing

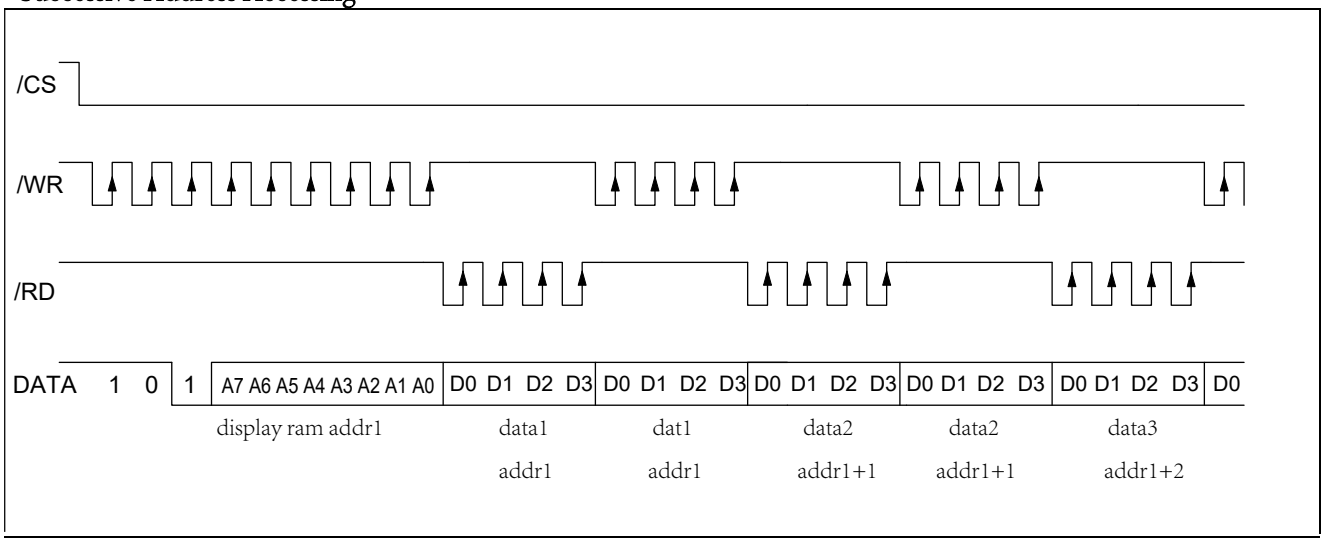


4.5.3.3 Read-Modify-Write Mode

Command Code :101

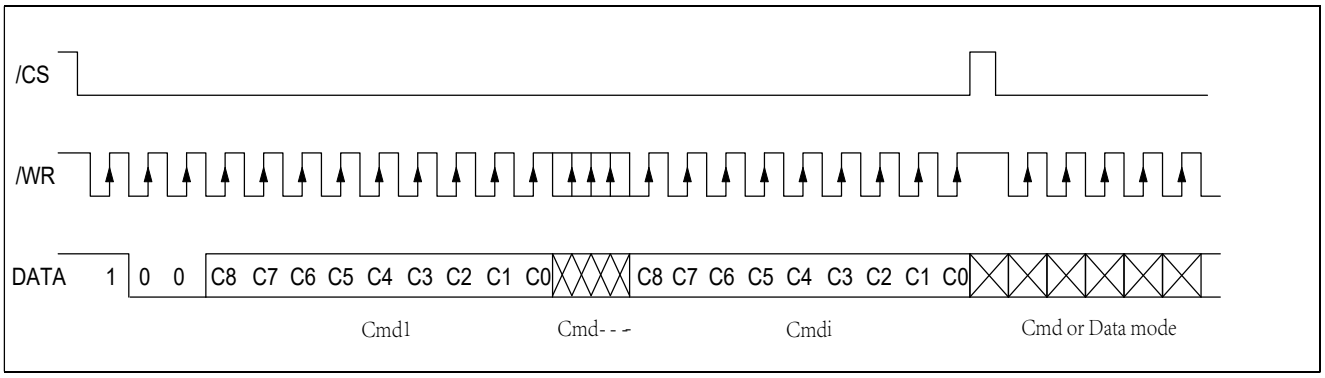


Successive Address Accessing



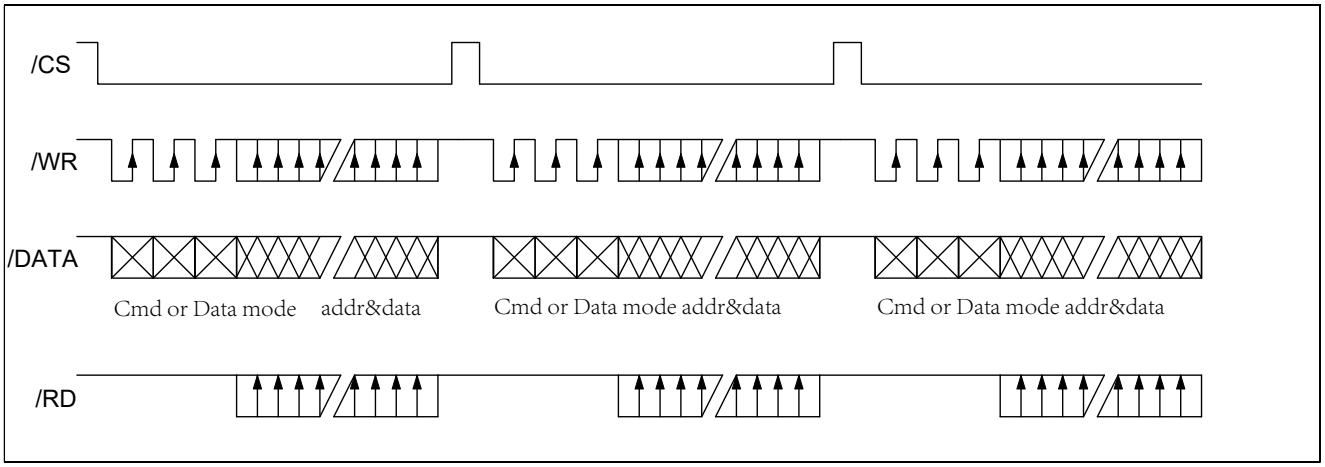
4.5.3.4 Command Mode

Command Code : 100



4.5.3.5 Data and Command Mode

Data and Command Mode



5 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A7A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A7A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A7A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000- 0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000- 0001-X	C	Turn on system oscillator	
LCD OFF	100	0000- 0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000- 0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000- 0100-X	C	Disable time base output	
WDT DIS	100	0000- 0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000- 0110-X	C	Enable time base output	
WDT EN	100	0000- 0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000- 1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC 32k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

note: : X: 0 or 1

A6-A0: Display RAM addresses

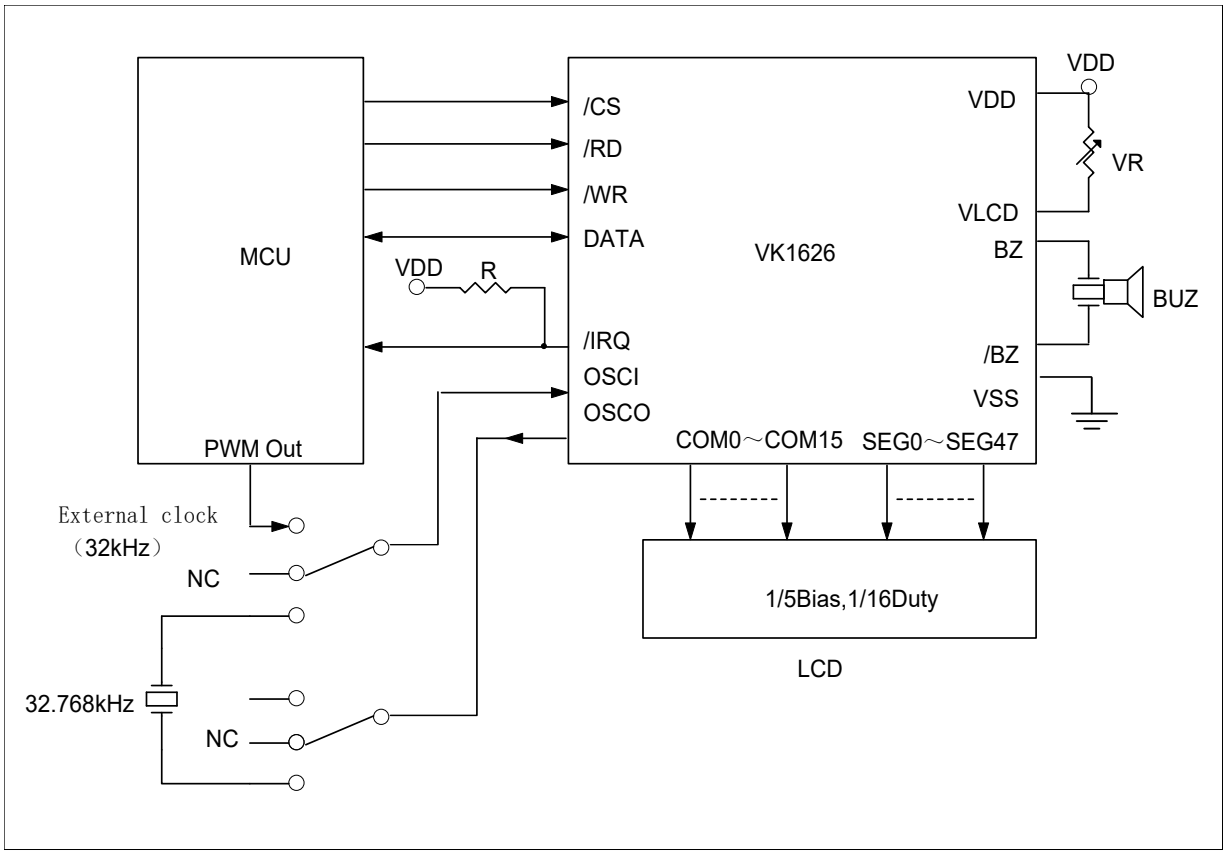
D3-D0:4bit Display RAM data

D/C:Data/Command mode

Def.:Power on reset default

110,101 and 100 is Command ID

6 Application Circuits



Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

7 Electrical characteristics

7.1 Absolute Maximum Ratings

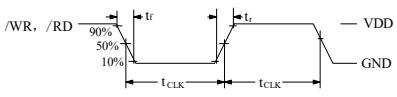
Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	VSS-0.3～VDD+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	TOTG	-40～+85	℃

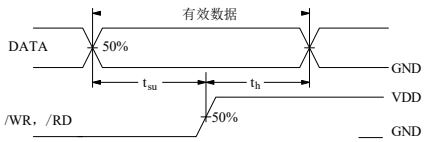
7.2 DC Characteristics

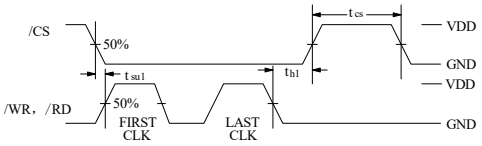
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	155	310	μA	3V	No load/LCD ON On-chip RC oscillator
		—	260	420		5V	
Operating current	I_{DD2}	—	150	310	μA	3V	No load/LCD ON External crystal
		—	250	420		5V	
Operating current	I_{DD11}	—	8	30	μA	3V	No load/LCD OFF On-chip RC oscillator
		—	20	60		5V	
Operating current	I_{DD22}	—	—	20	μA	3V	No load/LCD OFF External crystal
		—	—	35		5V	
Standby Current	I_{STB}	—	1	10	μA	3V	No load, Power down mode
		—	2	20		5V	
Input Low Voltage	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS, /RD
		0	—	1.0		5V	
Input High Voltage	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS, /RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	I_{OL1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
BZ, /BZ	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
DATA	I_{OL1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
DATA	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	160	—	μA	3V	V_{OL}=0.3V
		180	360	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-40	-80	—	μA	3V	V_{OH}=2.7V
		-90	-180	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	50	100	—	μA	3V	V_{OL}=0.3V
		120	240	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-30	-60	—	μA	3V	V_{OH}=2.7V
		-70	-140	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	100	200	300	kΩ	3V	DATA, /WR, /CS, /RD
		50	100	150		5V	

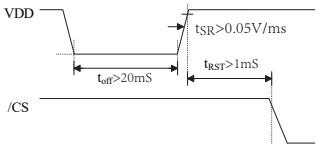
7.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	22	32	40	kHz	3V	On-chip RC oscillator
		24	32	40		5V	
System Clock	f_{SYS2}	—	32	—	kHz	3V	External clock source
		—	32	—		5V	
LCD Clock	f_{LCD1}	44	64	80	Hz	3V	On-chip RC oscillator
		48	64	80	Hz	5V	
	f_{LCD2}	—	64	—	Hz	3V	External clock source
		—	64	—	Hz	5V	
LCD Common Period	t_{COM}	—	N/ f_{LCD}	—	sec	—	N: Number of COM
Serial Data Clock (/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock (/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	



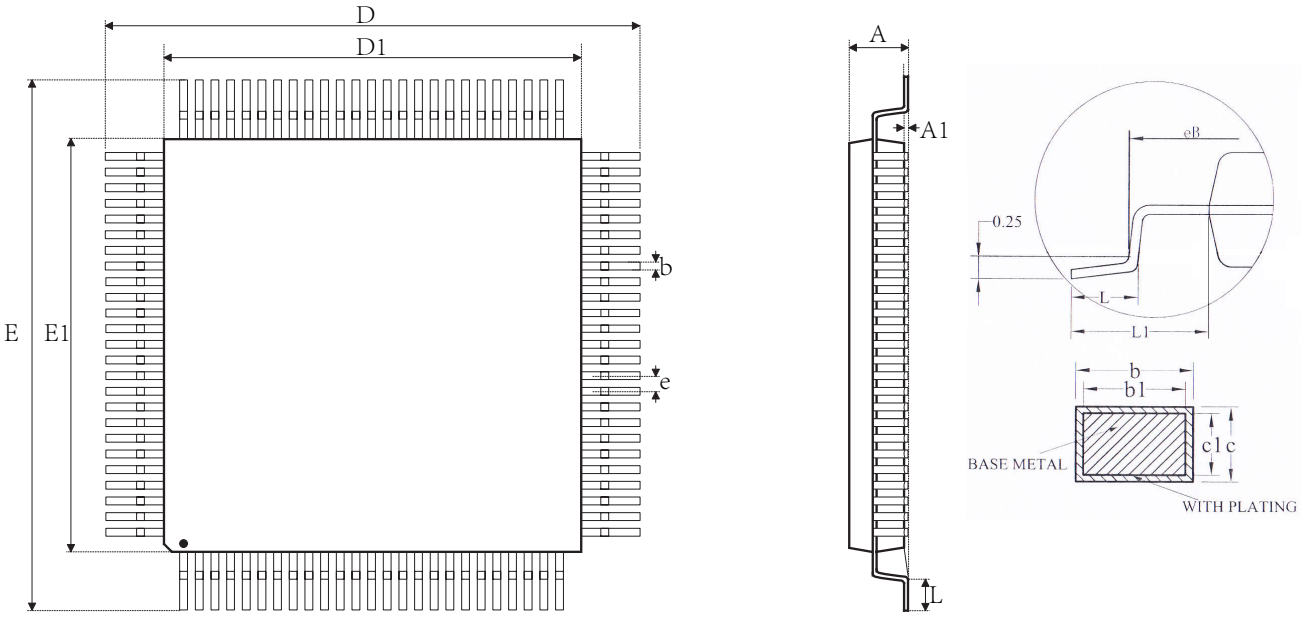






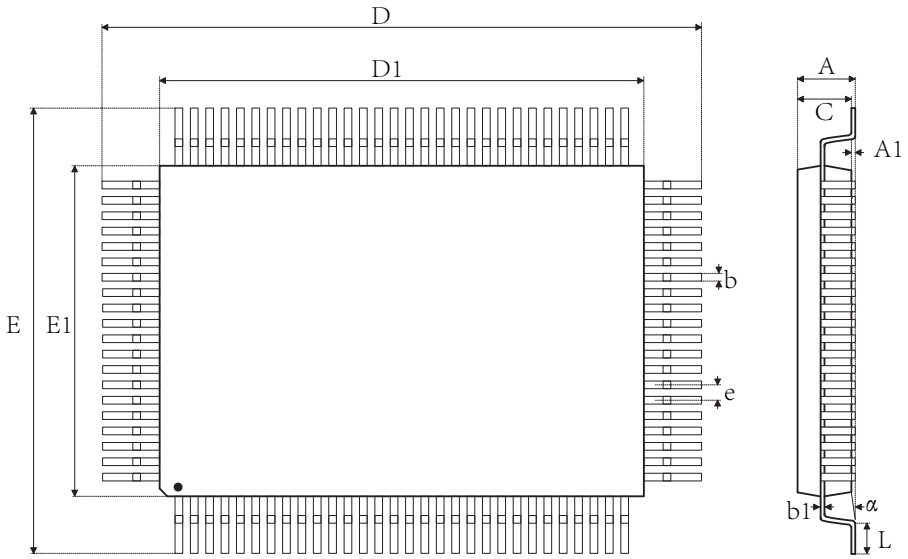
8.1 Package Information

8.1 LQFP100(14.0mm x 14.0mm PP=0.5mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		

8.2 QFP100(20.0mm x14.0mm PP=0.65mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	3.40
A1	0.25	--	0.50
b	--	0.3	--
b1	0.10	--	0.20
C	2.57	2.72	2.87
D	23.65	23.90	24.15
D1	19.90	20.00	20.10
E	17.65	17.90	18.15
E1	13.90	14.00	14.10
α	0°	--	7°
e	0.65BSC		
L	0.65	0.80	0.95

9 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

Disclaimers

Information in this document is believed to be accurate and reliable. However, VinKa does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. VinKa reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. For the latest information, please visit https://www.szvinka.com Or contact VinKa's staff.