Features

- Operating voltage 3.0-5.5V
- Built-in RC oscillator
- 8 SEG and 16 GRID（GRID numbers can be select 1 to 16）
- SEG pins connect to LED Anode , GRID pins connect to LED Cathode
- I2C bus interface
- 16-level brightness control（SEG constant current setting level 1 to 16）
- Dispaly mode 8x16
- Power-On Reset(POR)
- Output constant current
- Large driving current, suitable for highlight applications
- Package:
  SOP28(300mil)(18.0mm x 7.5mm PP=1.27mm)

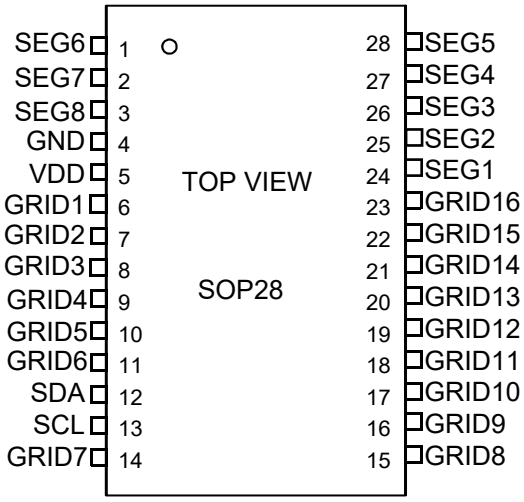
1 General Description

VK16D33 is a high accuracy constant current and RAM mapping LED display driver. The maximum display capacity of the devices is 128 patterns composed of 8 SEGs and 16 GRIDs. The devices can generate a 16 brightness levels using software config SEG output current. The devices provide constant current output control using software controlled for each SEG output terminal. A I2C interface is provided to allow the devices to receive instructions for its command mode and data mode. SEG pin is connected to LED anode and GRID pin is connected to LED cathode, which can support dot matrix LED display panels from 8SEGx1GRID to 8SEGx16GRID(software configuration), It is suitable for small LED. SOP28 Package.

Compared with the traditional LED display panel driver IC, when the number of LEDs changes or the input voltage changes, the current of a single LED will change, and can also enter the shutdown mode State control command（bit0=0） .which will affect the display brightness; The constant current design is adopted. When the display mode is configured, the current of each LED is constant and will not fluctuate due to the change of the number of lit LEDs and the change of input voltage.

2 Pinouts and pin description

2.1 VK16D33 SOP28 Pin Assignment

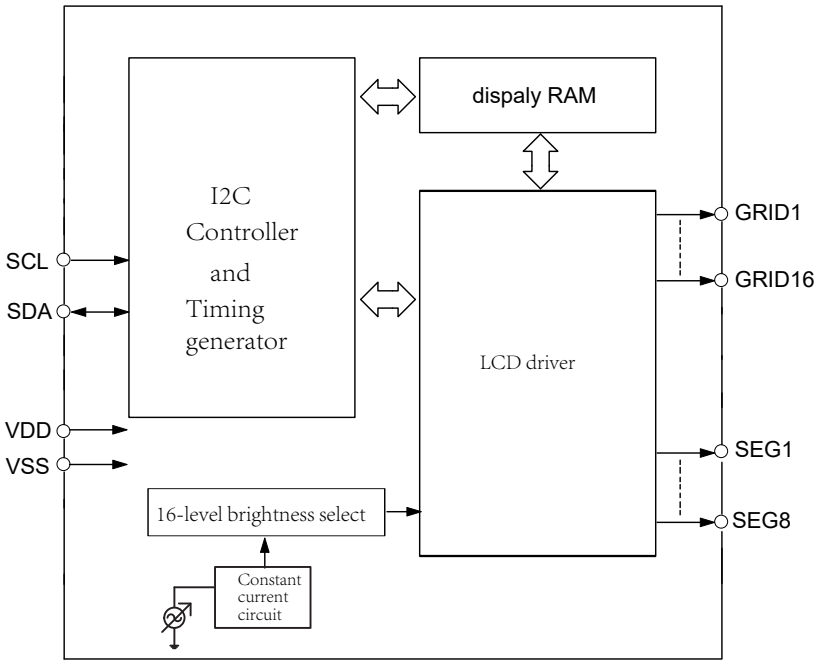


2.2 VK16D33 SOP28 Pin Description

No.	Name	I/O	Function
24~28 1~3	SEG1~SEG8	O	LED SEG outputs
4	GND	GND	Negative power supply
5	VDD	VDD	Positive power supply
6~11 14~23	GRID1 ~GRID6 GRID7 ~GRID16	O	LED GRID outputs
12	SDA	I/O	Serial Data Input/Output for I2C interface
13	SCL	I	Serial Clock Input for I2C interface

3 Functional Description

3.1 Block diagram



3.2 Display RAM

The static display memory (RAM) is organized into 8×16 bits and stores the displayed data.The contents of the RAM are directly mapped to the contents of the LCD driver. Display address is 0x00-0x0F,the RAM size is 16 bytes.If you want to lighted on or off an LED, only set or clear the corresponding display RAM bit to 1 or 0,For example, if LED1 driven by SEG0 pin and GRID1 pin is on or off, only set bit0 to 1 or 0 of the corresponding display RAM (0x00).The ram bit corresponding to the unused SEG pin is cleared to 0.

The following is a mapping from the RAM to the LED pattern:

SEG / GRID	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr
GRID1								LED1	0x00
GRID2									0x01
GRID3									0x02
GRID4									0x03
GRID5									0x04
GRID6									0x05
⋮				⋮					⋮
GRID14									0x0D
GRID15									0x0E
GRID16									0x0F
	D7	D6	D5	D4	D3	D2	D1	D0	

Note:

At the initial system power on, the value stored in the chip display RAM may be random. It is recommended to clear the display RAM after power on, write 0x00 to the all display RAM (0x00-0x0f).

SEG pins connect to LED Anode, GRID pins connect to LED Cathode, Reverse connection is not allowed.

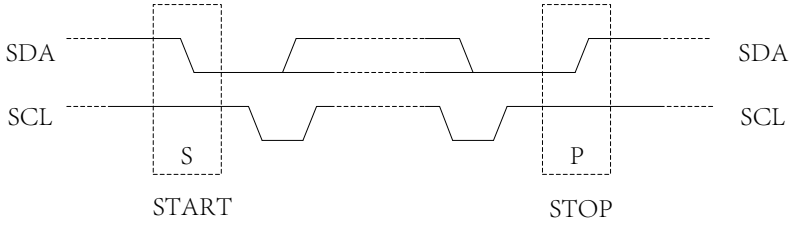
3.3 I2C Communication Command

3.3.1 I2C Serial Interface

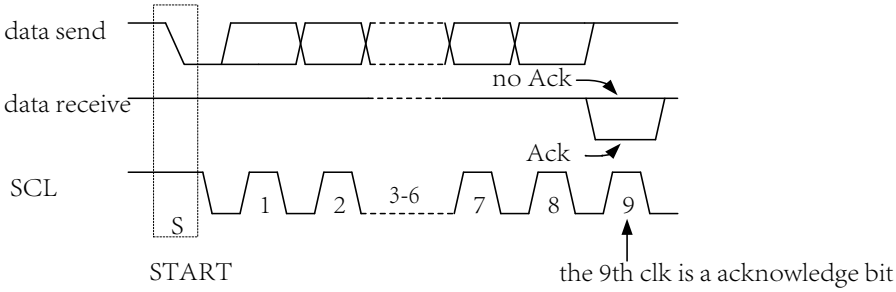
The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.

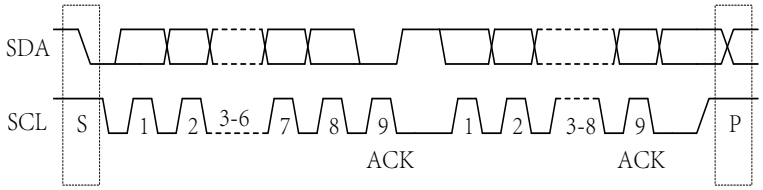
START and STOP



Acknowledge



Byte Format



Slave Address

(0x84) bit0-R/W

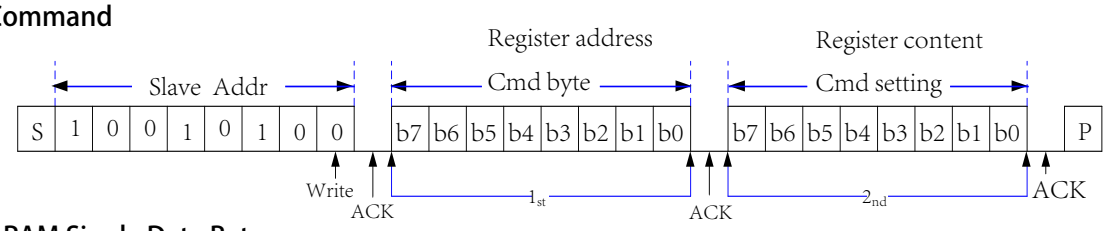
1	0	0	0	0	1	0	0

VK16D33 has two Slave addresses to select.
When ADDR is connected to VDD, the Slave address is 0x86;
When ADDR is connected to GND, the Slave address is 0x84. (default)
in the SOP28 package, the ADDR pin is not sealed out.

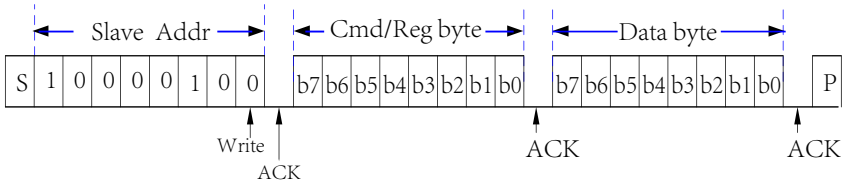
3.3.2 I2C Command Format

Write Operation

Write Command

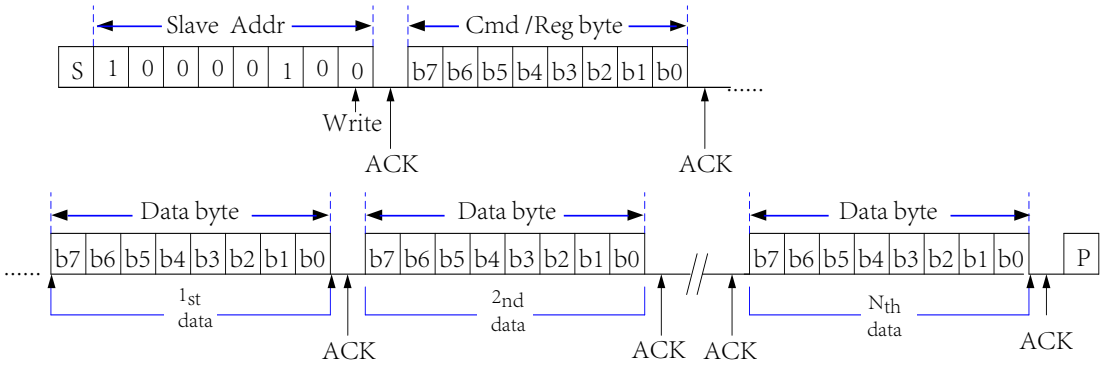


Display RAM Single Data Byte



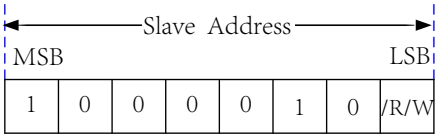
Note: If the byte after the slave address is a command byte, the byte after the command is ignored.

Display RAM Page Write Operation



3.3.3 Command Description

Slave Address
(0x84) bit0-R/W



After power on, the status control command （register 0x12) needs to be configured to 0x01 (work state).
Command(Register) writing sequence:
State control command → Display data command → Display control command → status control command.
Note: Once bit0 of the State control register is configured as "0", when rewriting data, be sure to configure the State control register to 0x01 before performing other operations.

3.3.3.1 Display Control Command

Set the Display brightness (level 16).

Register Address	Register content								Function
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Display brightness level (SEG continuous current))
0x10	--------- 0				1	1	1	1	70mA(default)
					1	1	1	0	65.6mA
					1	1	0	1	61.3mA
						-----			-----
					0	0	0	1	8.75mA
					0	0	0	0	4.37mA

Select number of scan GRID ,default 16GRID.

Register Address	Register content								Function
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	number of scan GRID
0x11	--------- 0				1	1	1	1	16GRID(default)
					0	0	0	1	15GRID
					0	0	1	0	14GRID
					-----				-----
					0	0	0	0	1GRID

3.3.3.2 State control command

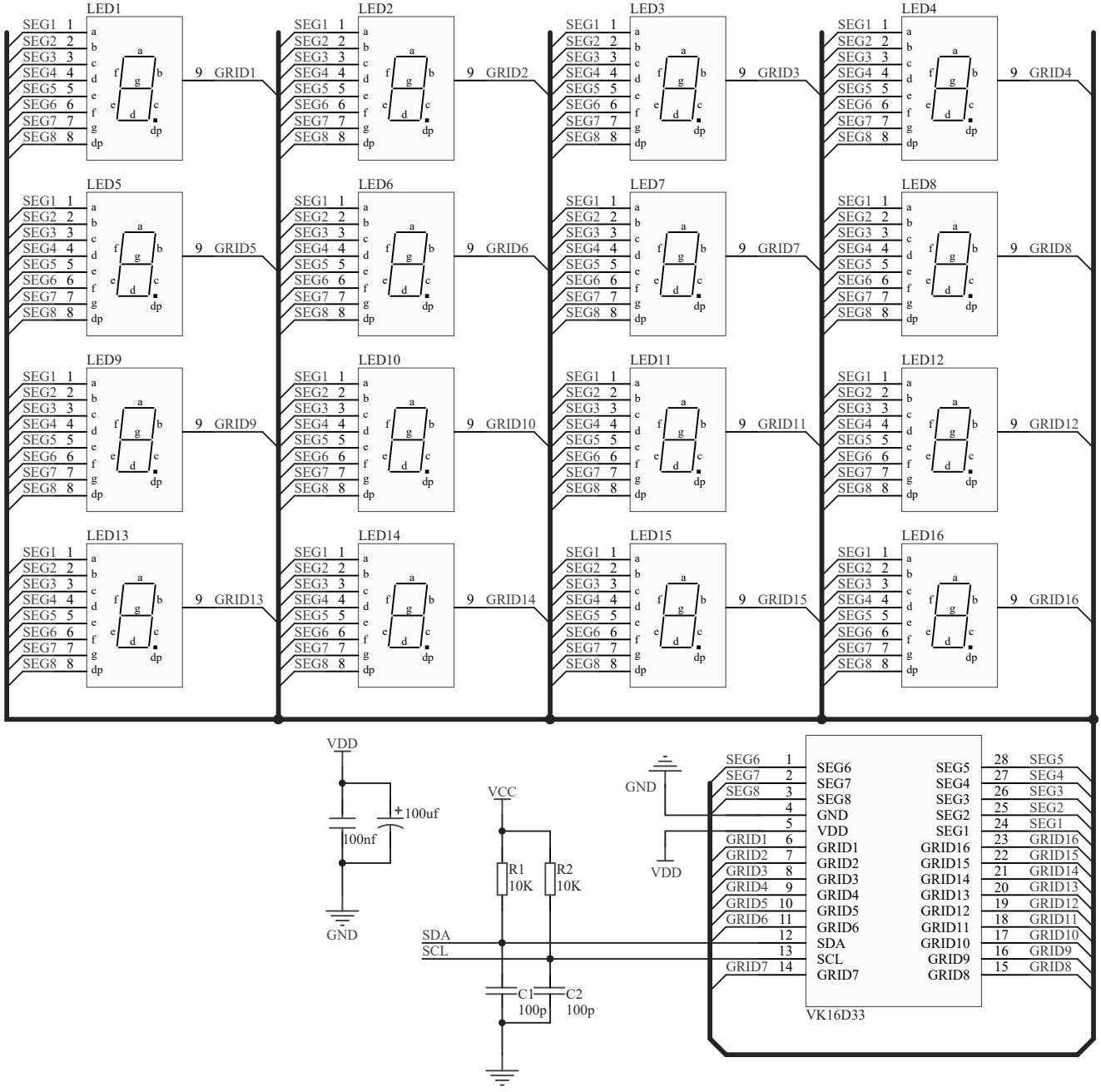
Register Address	Register content								Function
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	work state
0x12	--------- 0							0	Shutdown(default)
								1	nomal mode
							0		display off(default)
							1		display on

3.3.3.3 Display data command

The display data address is from 0x00 to 0x0f(16 bytes), corresponding to the LED lights of the matrix connected to SEG and GRID pins respectively.

display data address	display content								Function
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	display dat
0x00-0x0F	x	x	x	x	x	x	x	x	1 bit control 1 LED (by 1SEG and 1 GRID)

4 Application Circuits



5 Electrical characteristics

5.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～6.0	V
Input Voltage	VIN	V_{SS}-0.5～V_{DD}+0.5	V
Drive Output Current	$I_{OLGRID}\sum^{1}_{16}$	+600	mA
	I_{OHSEG}	-77	mA
Power Dissipation	P_D	1500	mW
Storage Temperature	TSTG	-65～+150	℃
Operating Temperature	T_{OTG}	-40～+85	℃

5.2 DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High Level output Current	I_{OHSG}	Vo=V_{DD}-1V SEG1～SEG8	-63	-70	-77	mA
Low Level input Current	I_{OLGOUT}	Vo=0.8V	—	560	—	mA
Input Current	I_{IN}	VI=VDD， SDA，SCL	—	—	±1	uA
Input Low Voltage V_{IH}		SDA,SCL	0.7V_{DD}	—	5	V
Input High Voltage V_{IL}		SDA,SCL	0	—	0.3V_{DD}	V
Hysteresis voltage	V_H	SDA,SCL	—	0.35	—	V
Dynamic current loss	I_{DD_DYN}	Noload/LED OFF	—	—	1	mA
shutdown Current	I_{SHUT}	Shutdown ennable			10	uA

5.3 AC Characteristics

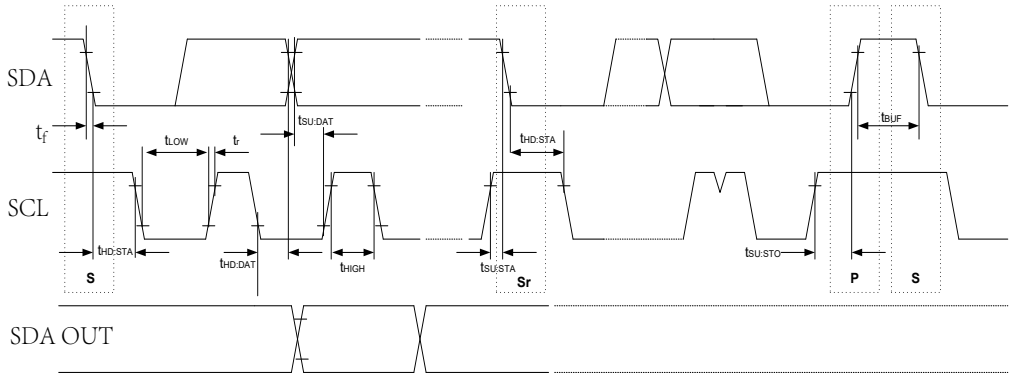
Switch Parameters

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Rising Time	T_{TZH1}	SEG1~8,CL=300pF	—	—	2	us
	T_{TZH2}	GRID1~16,CL=300pF	—	—	0.5	us
Falling Time	T_{TZH}	CL=300pF, SEGn, GRIDn	—	—	120	us

Timing Parameters

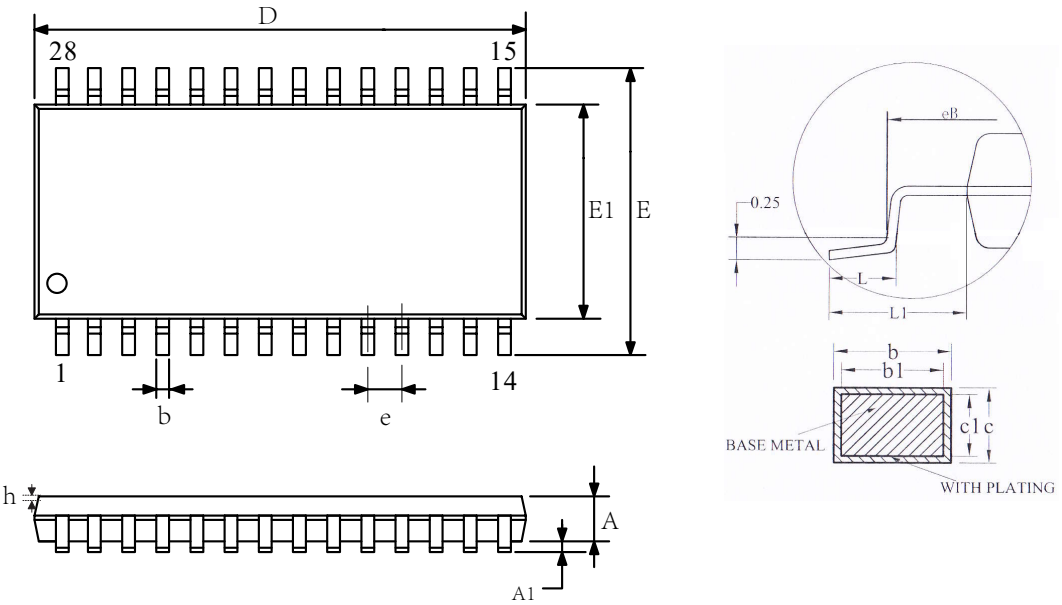
Symbol	Item	Min.	Typ.	Max.	Unit	Test Conditions
Clock Frequency	F_{SCL}	-	-	400	KHz	—
Bus Free Time	t_{BUF}	1.3	-	-	μS	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	-	μS	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	-	-	μS	—
SCL High Time	t_{HIGH}	0.6	-	-	μS	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	-	μS	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	-	-	0.9	nS	—
Data Setup Time	$t_{HD:DAT}$	100	-	-	nS	—
SDA , SCL Rising Time	t_R	20+0.1Cb[1]	-	-	nS	periodically sampled
SDA,SCL Falling Time	t_F	20+0.1Cb	-	-	nS	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	-	-	-	μS	—

I^2C Timing



6 Package Information

6.1 SOP28 (300mil) (18mm x 7.5mm PP=1.27mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	2.65
A1	0.10	--	0.30
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.25	--	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.30	--	0.50
L	0.70	--	1.00
L1	1.40REF		

7 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2019-07-11	Add Ref circuits	Yes
3	1.2	2020-02-11	Update content	Yes

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