Features

- Operating voltage 3.0-5.5V
- Built-in RC oscillator
- 10 SEG pins,4 GRID pins,3 SEG/GRID multiplex pins
- SEG pins connect to LED Anode , GRID pins connect to LED Cathode
- 10x2 matrix keys, support multiple keys (key / display multiplexing requires hardware circuit)
- 3-wire serial interface
- 8-level brightness control
- Built-in 14×8 bit display RAM
- Power-On Reset(POR)
- Strong anti-interference ability

- Package:.

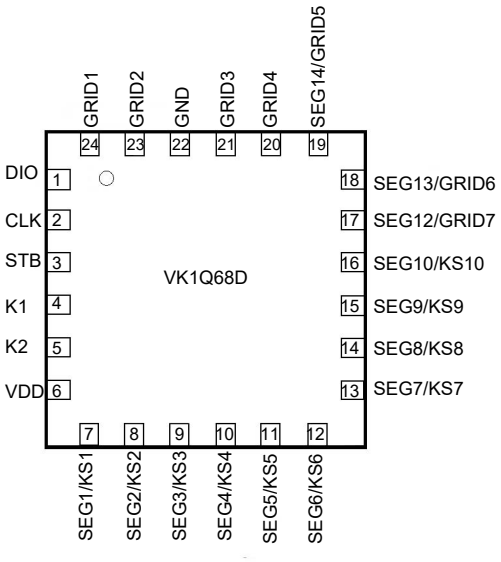
  QFN24L(4mmX4mm×0.75mm-0.50mm)

1 General Description

VK1Q68D is a RAM Mapping LED display driver with key scan，The Display segment numbers in the device can be select as 13SEGx4GRID、12SEGx5GRID、11SEGx6GRID、10SEGx7GRID, with a 10×2 (MAX.) matrix key scan circuit .it suitable for multiple LED applications including LED modules and display subsystems. The device communicates with host microcontrollers via a 3 line Serial Interface,it is used to configure display parameters and transfer display data. QFN24L package.

2 Pinouts and pin description

2.1 VK1Q68D QFN24L Pin Assignment

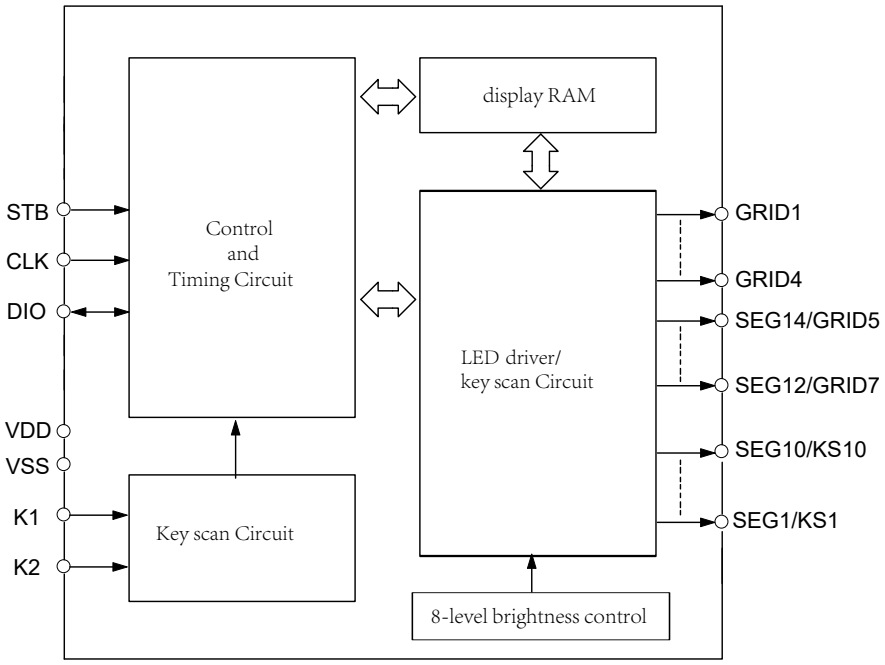


2.2 VK1Q68D QFN24L Pin Assignment

No.	Name	I/O	Function
1	DIO	I/O	Bidirectional data pin (NMOS open drain), data input / output from low bit. Read the data of the DIO pin to the display RAM at the rising edge of the CLK, and output the data to the DIO pin at the falling edge of the CLK.
2	CLK	I	CLK signal input pin, reads the data of the DIO pin to the display RAM on the rising edge, and outputs the data to the DIO pin on the falling edge.
3	STB	I	Chip selection signal input pin, 1-disabe，0-enable.
4，5	K1,K2	I	KEY scan input, the key signal is locked after the end of the display cycle
6	VDD	VDD	Positive power supply
7-16	SEG1/KS1-SEG10/KS10	O	LED SEG outputs（P-MOS open drain）；Key scan output
17,18 19	SEG12/GRID7-SEG14/GRID5	O	LED SEG/COM multiplex output, configured by software
23，24 26，27	GRID4-GRID1	O	LED GRID outputs（N-MOS open drain）
22	VSS	VSS	Negative power supply

3 Functional Description

3.1 Block diagram



3.2 Display RAM

The static display memory (RAM) is organized into 14×8 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Display address is 0xC0-0xCD. ,the RAM size is 14 bytes. If you want to lighted on or off an LED, only set or clear the corresponding display RAM bit to 1 or 0,For example, if LED1 driven by SEG1 pin and GRID1 pin is on or off, only set bit0 to 1 or 0 of the corresponding display RAM (0xc0).The ram bit corresponding to the unused SEG pin is cleared to 0.

The following is a mapping from the RAM to the LED pattern:

SEG / GRID	X	X	SEG14	SEG13	SEG12	X	SEG10	SEG9	Address	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Address	SEG / GRID
GRID1									0xC1								LED1	0xC0	GRID1
GRID2									0xC3									0xC2	GRID2
GRID3									0xC5									0xC4	GRID3
GRID4									0xC7									0xC6	GRID4
⋮									⋮									⋮	⋮
GRID7									0xCD									0xCC	GRID7
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

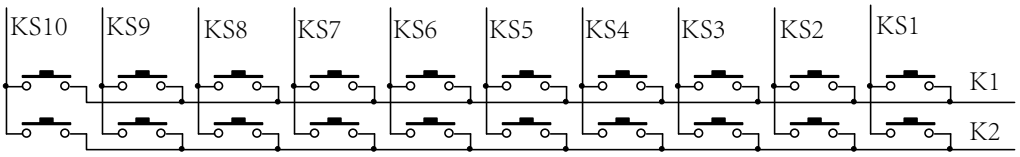
Note:

At the initial system power on, the value stored in the chip display RAM may be random. It is recommended to clear the display RAM after power on, write 0x00 to the all display RAM (0xc0-0xcd).

SEG pins connect to LED Anode, GRID pins connect to LED Cathode, Reverse connection is not allowed.

3.3 Keyscan

3.3.1 Key data reading



The keys scanning is automatically completed by the hardware, only needs to read the key value through serial interface.Two display cycles are required to complete a key scan. One display cycle takes about 4ms. If two different keys are pressed successively within 8ms, the two key value is the key pressed first.

After sending the read key command, start reading 5 bytes of key data in sequence, and read key data is output from the low bit. When a key is pressed, the corresponding bit of the key data byte is set 1.

The following shows the mapping from the RAM to the key data output:

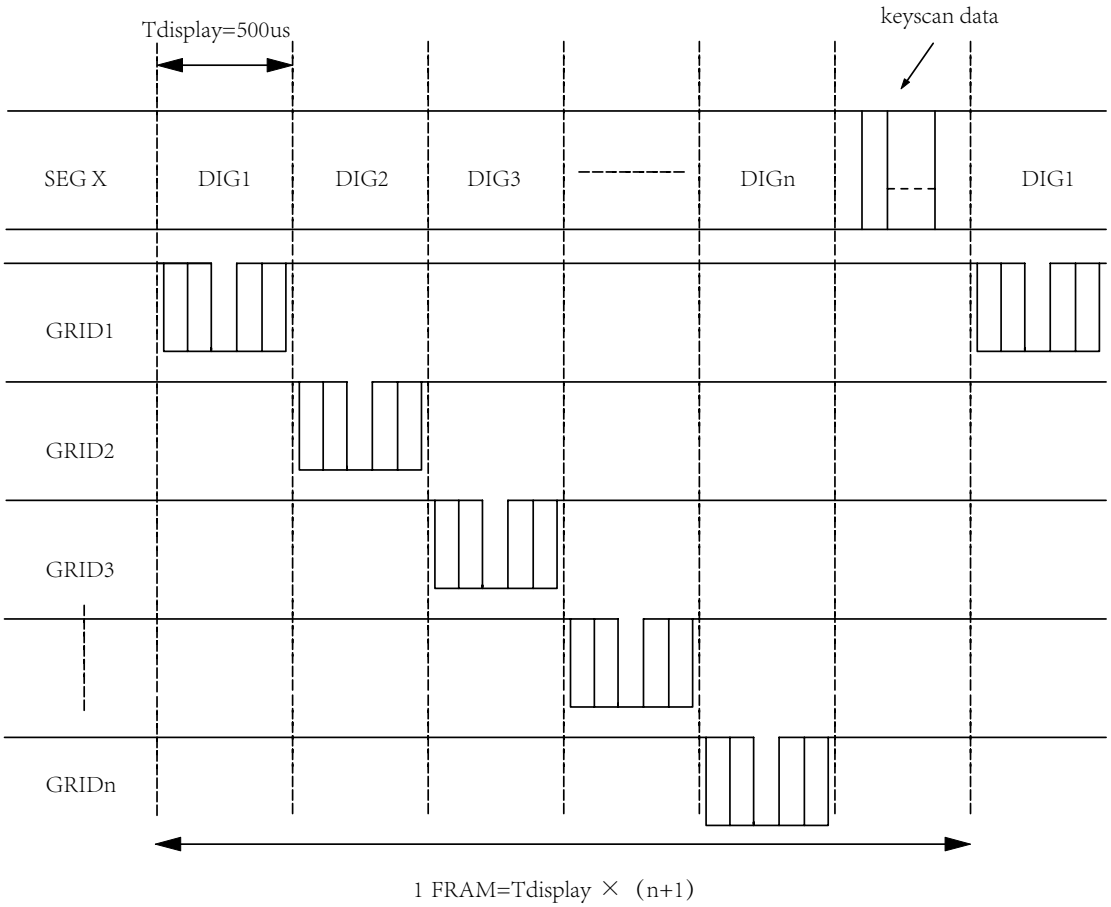
key data	X	X	X	K2	K1	X	K2	K1
byte0	0	0	0	K2/KS2	K1/KS2	0	K2/KS1	K1/KS1
byte1	0	0	0	K2/KS4	K1/KS4	0	K2/KS3	K1/KS3
byte2	0	0	0	K2/KS6	K1/KS6	0	K2/KS5	K1/KS5
byte3	0	0	0	K2/KS8	K1/KS8	0	K2/KS7	K1/KS7
byte4	0	0	0	K2/KS10	K1/KS10	0	K2/KS9	K1/KS9
	D7	D6	D5	D4	D3	D2	D1	D0

Note： The key data must be read in sequence, not across bytes, and not more than 5 bytes.

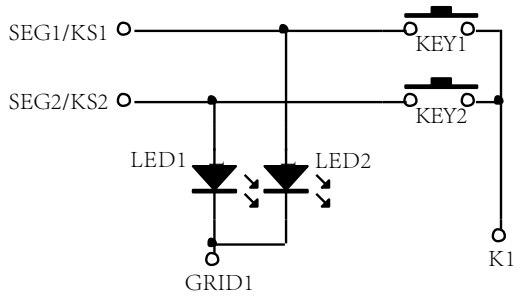
3.3.2 Keyscan Timing

One cycle of key scanning includes two frames, the first frame displays the cycle scanning keys KS1-KS8, and the second frame displays the cycle scanning keys KS9-KS10, The data of 10 x 2 matrix key is stored in RAM.

keyscan timing as shown:

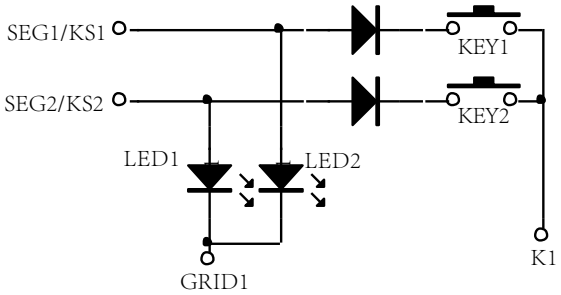


3.3.3 Key/display multiplexing



For example, if LED1 On, LED2 Off,It need to set SEG1="0" and SEG2 ="1".When KEY1 and KEY2 are pressed at the same time, SEG1 and SEG2 are short circuited, and if LED1 On, LED2 Off,It need to set SEG1="0" and SEG2 ="1".When KEY1 and KEY2 are pressed at the same time, SEG1 and SEG2 are short circuited, and LED1/LED2 On.It can be solved by connecting diodes in series at SEG1 and SEG2 pins.

As shown below:



3.4 Serial communication command

3.4.1 Serial Interface

3 lines are required to interface with the VK1Q68D.

STB is the chip select pin.it is used to enable / disable communication with the controller, high level disable(prohibits and initializes internal timing), low level enables. The first byte input by the DIO pin after the falling edge of the STB is used as the command. If the STB is set to high level during instruction or data transmission, the serial communication is initialized and the command or data being transmitted is invalid.

CLK is the clock signal pin. It reads the data of DIO pin to display RAM on the rising edge and outputs the data to DIO pin on the falling edge.

DIO is the Bidirectional data pin. It used to read / write data or write commands . it is an NMOS open drain output and needs to connect a resistor. with VDD

3.4.2 Command Format

Command is used to set the Display Mode or write the Display Data or read Key data. After the falling edge of STB, the first byte input by DIO is used as the command byte, After decoding, Bit7 and bit6 of the byte are the command bits, as shown in the following table:

bit7	bit6	Command Function
0	0	Display Mode Set Command
0	1	Data Read/Write Set Command
1	0	Display Control Command
1	1	Address Set Command

3.4.3 Command Description

3.4.3.1 Display Mode Set Command

Set the number of SEGs and GRIDs (4 ~ 7GRIDs, 10 ~ 13SEGs). When the command is executed, Forced display off. If the same mode setting is selected, the command will not be executed.

When powered on, the default display mode is 10 SEGs and 7 GRIDs.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Display Mode
0	0	---				0	0	13SEG 4GRID
0	0					0	1	12SEG 5GRID
0	0					1	0	11SEG 6GRID
0	0					1	1	10SEG 7GRID

3.4.3.2 Data Read/Write Set Command

This command is used to write Display data and related commands. Bit1 and bit0 bits are not allowed to be set to 01 or 11.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
0	1	---				0	0	Read/Write data	Write data to the RAM
0	1					1	0		Read keydata
0	1				0			Address mode set	address increase
0	1				1				address fixed
0	1			0				Work mode set	normal mode
0	1			1					test mode

3.4.3.3 Address Set Command

Set the address of the Display RAM (0xC0 - 0xCD). When powered on, the address is set to 0xC0(default).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	RAM Address
1	1	---		0	0	0	0	0xC0
1	1			0	0	0	1	0xC1
1	1			0	0	1	0	0xC2
1	1			0	0	1	1	0xC3
1	1			0	1	0	0	0xC4
1	1			0	1	0	1	0xC5
1	1			0	1	1	0	0xC6
1	1			0	1	1	1	0xC7
1	1			1	0	0	0	0xC8
1	1			1	0	0	1	0xC9
1	1			1	0	1	0	0xCA
1	1			1	0	1	1	0xCB
1	1			1	1	0	0	0xCC
1	1			1	1	0	1	0xCD

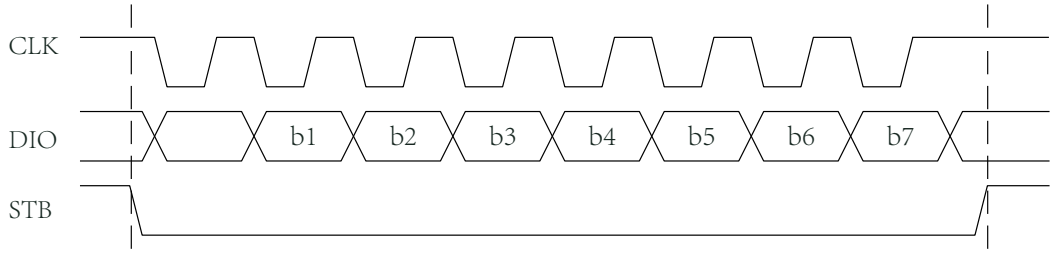
3.4.3.4 Display Control Command

Set the Display ON or OFF and select the Display brightness (level 8).

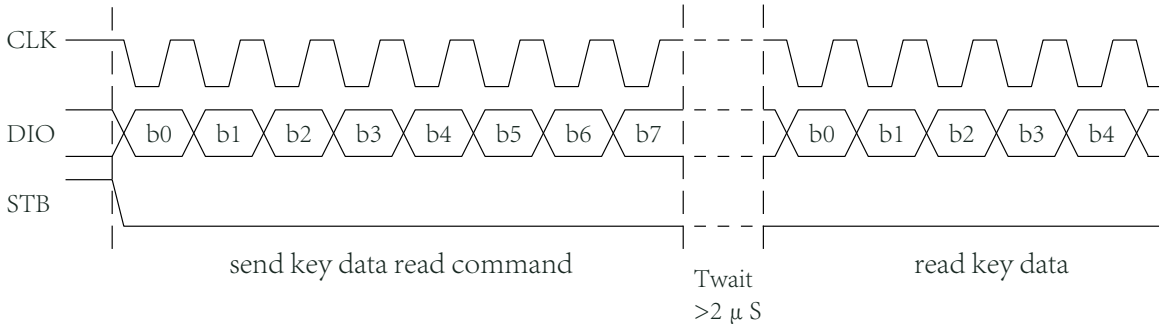
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
1	0	---			0	0	0	Set GRID Pulse Width	1/16 duty
1	0				0	0	1		2/16 duty
1	0				0	1	0		4/16 duty
1	0				0	1	1		10/16 duty
1	0				1	0	0		11/16 duty
1	0				1	0	1		12/16 duty
1	0				1	1	0		13/16 duty
1	0				1	1	1		14/16 duty
1	0			0				Display on/off	Display off
1	0			1					Display on

3.4.4 Command Timing Diagrams

Write command or display data



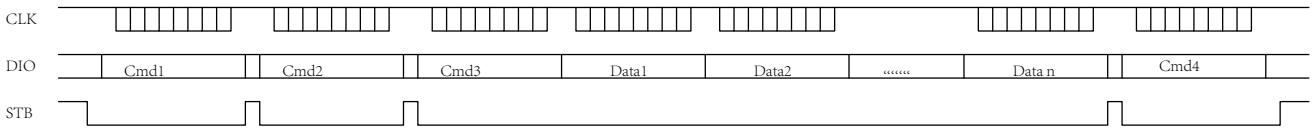
Read key data



4 Command application

4.1 Send Display data(Address auto Increment)

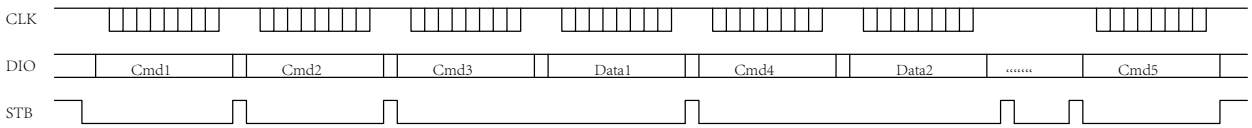
Using the address auto-increase mode,First set the starting address of the data to be transmitted (Display RAM address). After the start address command byte is sent, the display data is directly transmitted, up to 14 bytes.



Cmd1： Display Mode Set Cmd -Set the number of SEG and GRID displayed by the LED(Can be set at initialization)
Cmd2： Data Read/Write Set Cmd -Set address auto-increase mode （0x40）
Cmd3: Address Set Cmd -Set the start address of the display RAM （0xC0-0xCD）
Data1-Datan： Send display data to the start address set by Cmd3and the subsequent address (up to 14 bytes)
Cmd4： Display Control Cmd -Display ON and select the Display brightness

4.2 Send Display data(Fixed Address)

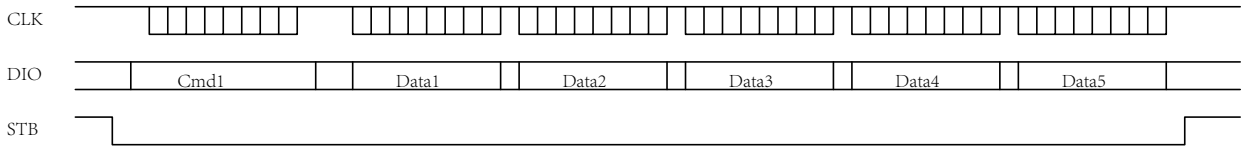
Using the fixed address mode, first set the address of the data to be transmitted (Display RAM address), After sending the address, directly transmit 1 byte of display data; Then transfer the address of the next display data, and directly transfer 1 byte of display data Until the last byte of display data is transmitted,Up to 14 bytes.



Cmd1： Display Mode Set Cmd -Set the number of SEG and GRID displayed by the LED(Can be set at initialization)
Cmd2： Data Read/Write Set Cmd -Set fixed address mode （0x44）
Cmd3： Address Set Cmd -Set Display RAM address （0xC0-0xCD）
Data1： Send the Display data to the display RAM address set by Cmd3
Cmd4： Address Set Cmd -Set Display RAM address （0xC0-0xCD）
Data2： Send the Display data to the display RAM address set by Cmd4
....up to 14 bytes of data to be send
Cmd5： Display Control Cmd -Display ON and select the Display brightness

4.3 Read Key Data

Data Read/Write Set Command is Set to read the key data, and then start reading the key data of 5 bytes in sequence. The read key data is output from the low bit.

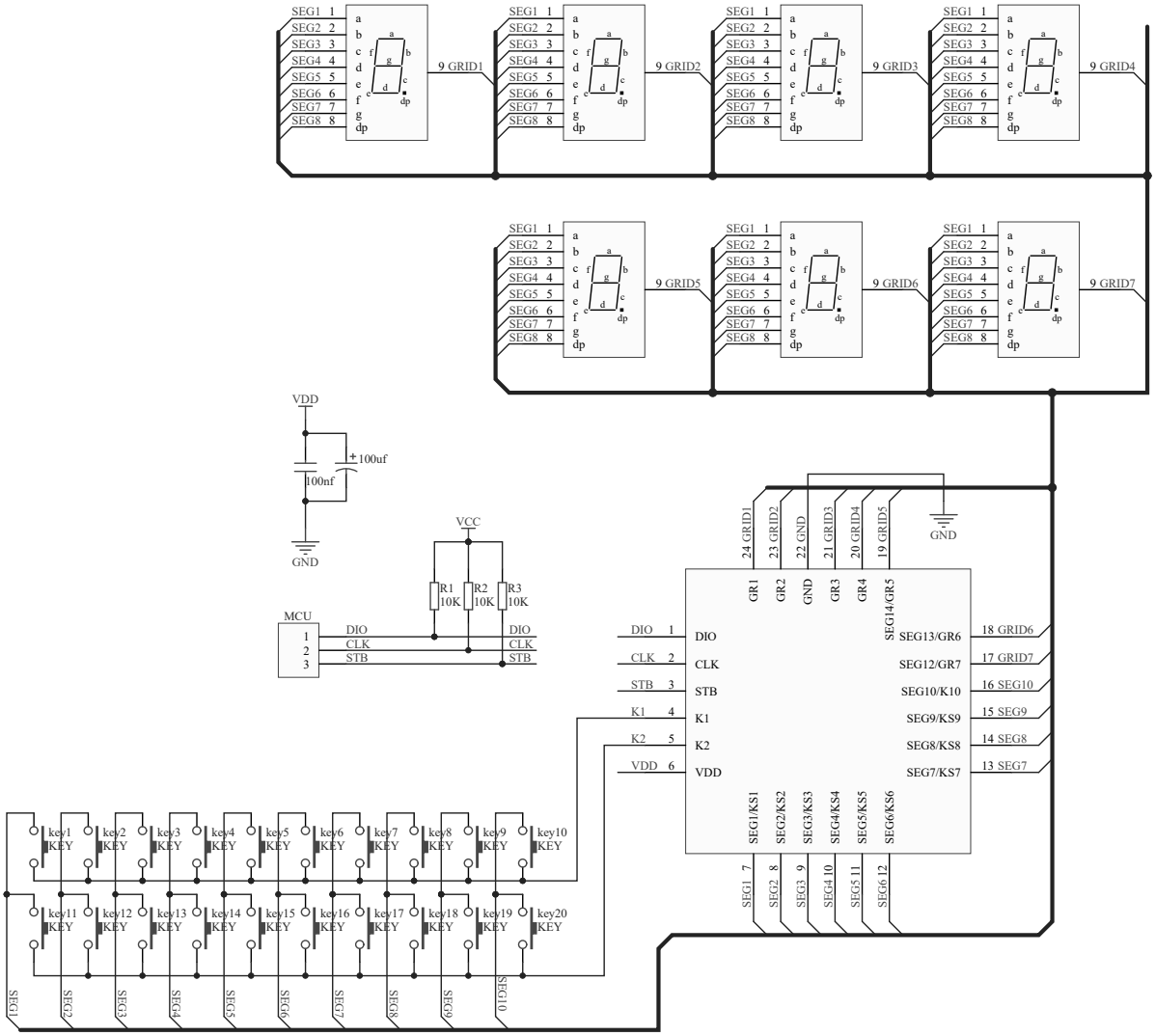


Cmd1： Data Read/Write Set Cmd -Set to read key data (0x42)

Data1-Data5： Read 5 bytes of key data in sequence, and the read key data is output from the low bit.

5 Application Circuits

8-SEG LED Display shared Cathode



6 Electrical characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～7.0	V
Input Voltage	VIN	V_{SS}-0.5～V_{DD}+0.5	V
Power Dissipation	PD	400	mW
Drive Output Current	I_{OLGRID}	+250	mA
	I_{OHSEG}	-50	mA
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

6.2 DC Characteristics

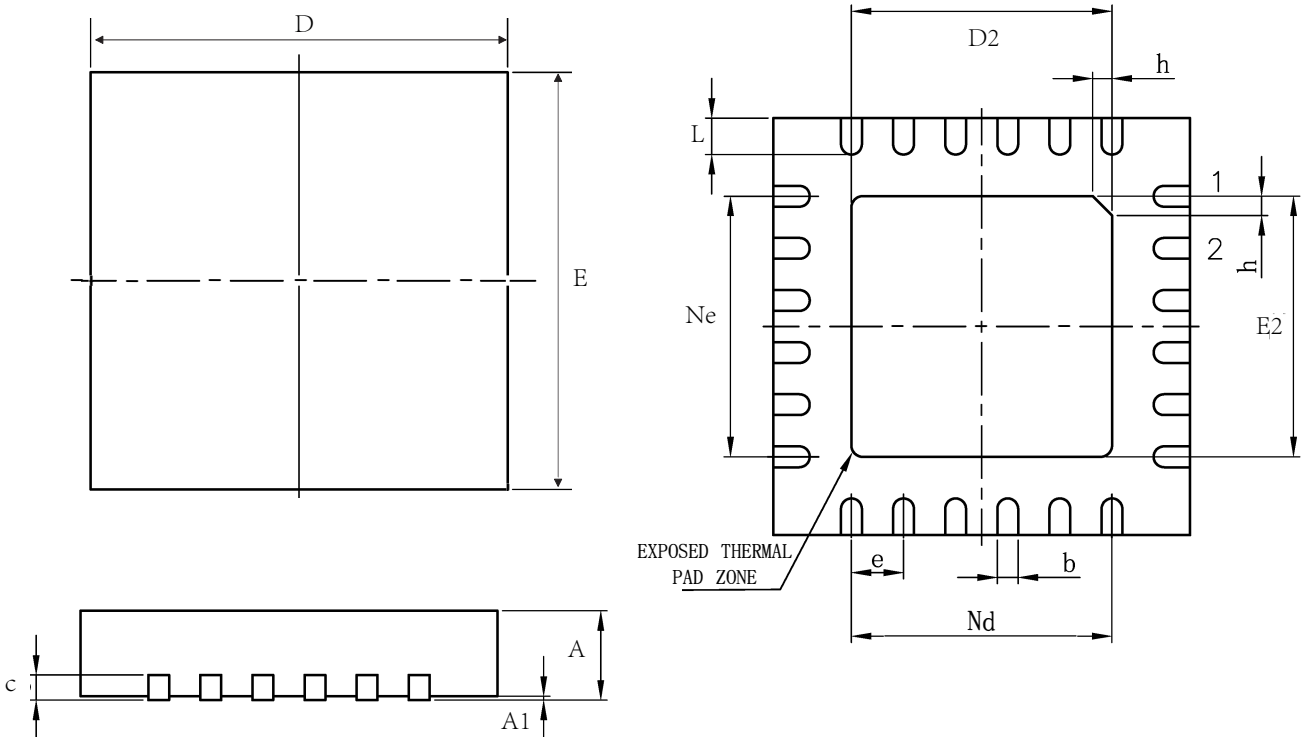
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating Voltage	VDD	3.0	—	5.5	V	—	—
Quiescent Current	I_{DD}	—	0.5	1.0	mA	5V	Noload/LED OFF
High Level output Current	I_{OHSEG1}	-20	-25	-40	mA	5V	VO=VDD-2V SEG1/KS1- SEG10/KS10 SEG12/GRID7-SEG14/GRID5
	I_{OHSEG2}	-25	-30	-50			VO=VDD-3V SEG1/KS1- SEG10/KS10 SEG12/GR7-SEG14/GR5
Low Level input Current	I_{OLGRID}	100	140	—	mA	5V	VO=0.3V GRID1- GRID4 SEG14/GRID5-SEG12/GRID7
High level output current tolerance	I_{TOLSEG}	—	—	5	%	VDD	VO=VDD-3V(VDD=5V) VO=VDD-2V(VDD=3V) SEG1/KS1 to SEG10/KS10, SEG12/GRID7 to SEG14/GRID5
Input Low Voltage	V_{IL}	0	—	0.3	VDD	VDD	STB, CLK, DIO
Input High Voltage	V_{IH}	0.7	—	1.0		VDD	
pull-down resistor	R_L	40	—	100	kΩ	5V	K1, K2

6.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Transmission delay time	t_{PLZ}	-	-	300	nS	CLK → DOUT CL = 15pF, RL = 10K Ω
	t_{PZL}	-	-	100	nS	
Rise Time	t_{ZH} 1	-	-	2	μS	CL=300pF SEG1-SEG10
	t_{TZH} 2	-	-	0.5	μS	CL=300pF GRID1-GRID4 SEG12/GRID7～SEG14/GRID5
Fall Time	t_{THZ}	-	-	1.5	μS	CL = 300pF SEGn,GRIDn
Max. input Freq	FMAX	-	-	1	MHz	50% duty
Input Capacitance	CI	-	-	15	pF	-

7 Package Information

7.1 QFN24L(4mmX4mm×0.75mm-0.50mm)



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2019-07-11	Add Ref circuits	Yes
3	1.2	2020-02-11	Update content	Yes

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