



VK0256 Datasheet

32×8 LCD DRIVER

Rev.1.3

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1 General Description

VK0256 is a dot-matrix storage-mapped LCD driver that supports LCD screens with a maximum of 256 dots (32SEG×8COM). The single-chip microcomputer can be configured to display parameters and send display data through a 3/4-wire serial interface, and can also enter power-saving mode through instructions.

2 Key Features

- Operating voltage:2.4-5.2V
- Integrated RC oscillator (default)
- External clock source: 32 kHz (OSCI)
- Selectable LCD bias:1/4
- Selectable LCD duty:1/8 duty
- Built-in 32×8 bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential read/write
- VLCD adjustable via external pin ($\leq VDD$)
- Available Packages:Package :
QFP64(20.0mm × 14.0mm PP=1.0mm)

3 Application field

- Electricity meter/gas meter
- Massage device/beauty device
- Medical instruments
- Vehicle-mounted equipment
- Air conditioner/heater

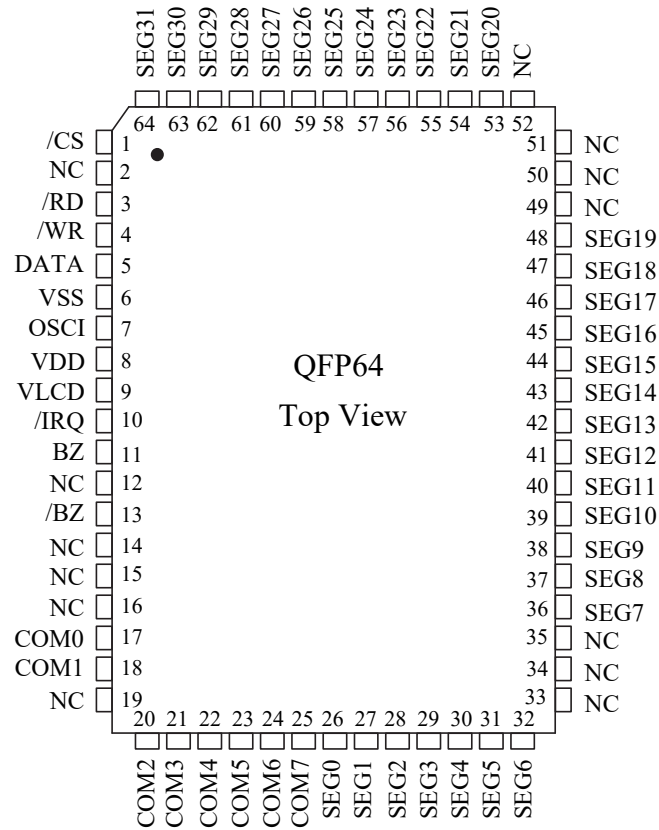
4 Product Selection

Part No.	VK0192	VK0256	VK0256B	VK0256C	VK0384
COM	8	8	8	8	8
SEG	24	32	32	32	48
On-chip oscillator	√	√	√	√	√
External clock	√	√	√	√	-

5 Ordering Information

Part No	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK0192	LQFP44	-	160/tray	1600/box	9600 PCS	
VK0256	QFP64	-	66/tray	660/box	3960 PCS	
VK0256B	LQFP64	-	250/tray	2500/box	15000 PCS	
VK0256C	LQFP52	-	90/tray	900/box	5400 PCS	
VK0384	LQFP64	-	250/tray	2500/box	15000 PCS	

6 Package Pinout Information(QFP64)



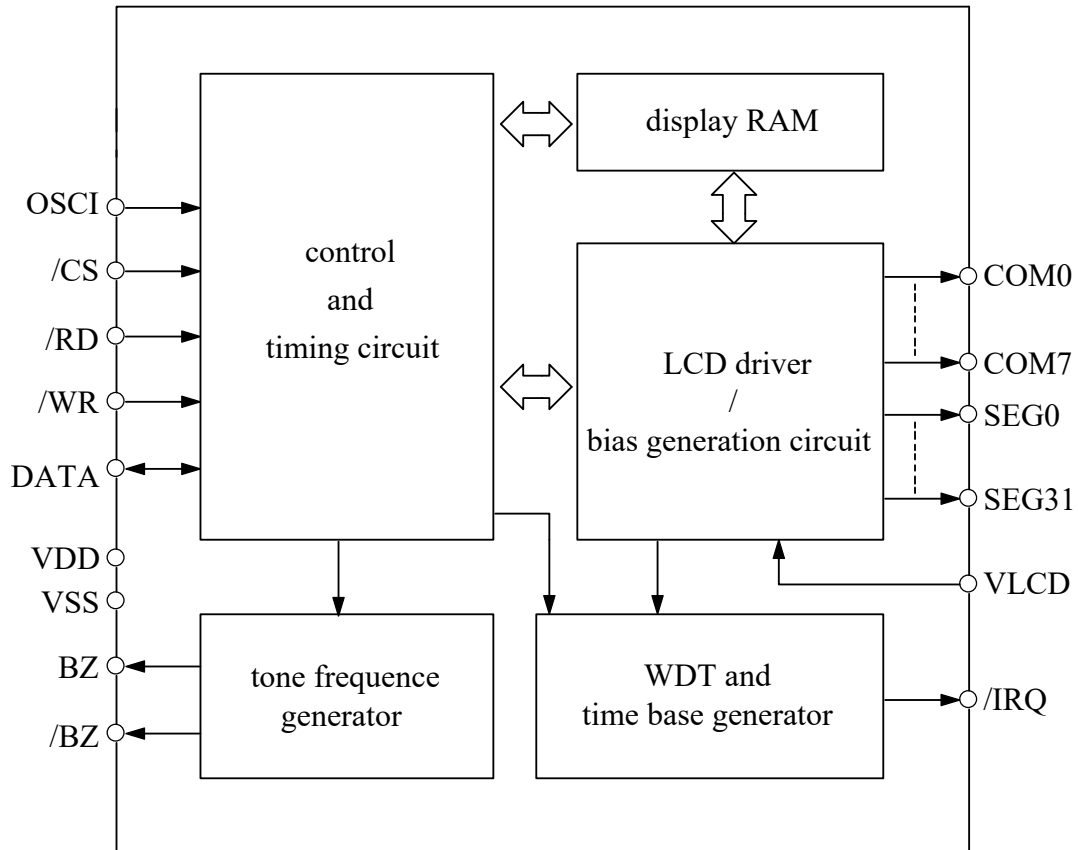
For more information: [Page 18](#)

6.1 VK0256/QFP64 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
3	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
4	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
5	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
6	VSS	VSS	Negative power supply
7	OSCI	I	External clock source: OSCI connect a external clock source When using the internal RC oscillator, it is suspended
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be \leq VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair, when TONE OFF the BZ and /BZ pins output low level.
13	/BZ	O	
14-16	NC	—	—
17,18 20-25	COM0-COM7	O	LCD COM drive outputs
26-32 36-48 53-64	SEG0-SEG31	O	LCD SEG drive outputs

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The VK0192 integrates 32×8 -bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0	
SEG0					1					0
SEG1					3					2
SEG2					5					4
SEG3					7					6
⋮					⋮					⋮
SEG31					63					62
	D3	D2	D1	D0	Data\Addr	D3	D2	D1	D0	Data\Addr

address 6 bit
(A5---A0)

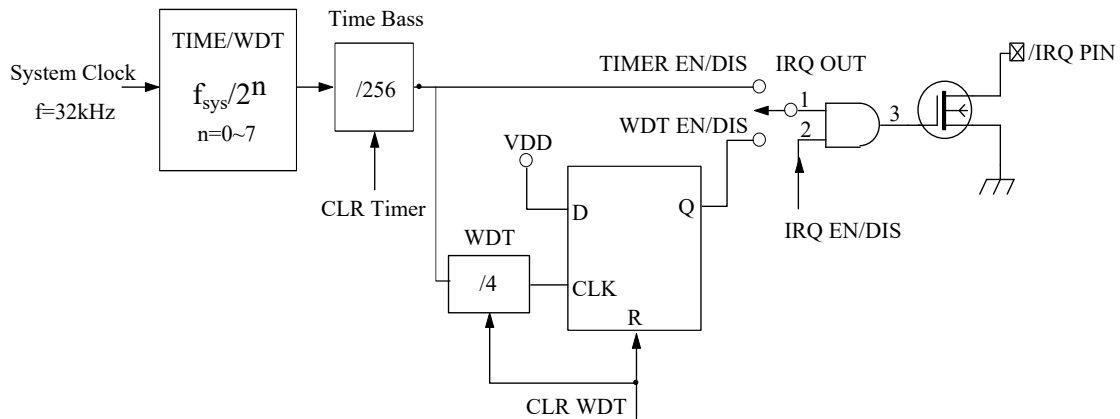
7.3 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{\text{WDT}} = f_{\text{sys}} / 2^n \quad (n=0 \sim 7) \quad f_{\text{sys}} = 32\text{kHz}$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively. By default, the /IRQ output is disabled upon system power-up

Timer and WDT Configurations:



7.4 Tone Output

The VK0256 integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

7.5 LCD Driver

The VK0256 is a 256-segment LCD driver (32SEG×8COM). It supports software-configurable bias settings of 1/4, and COM configurations of 8.

7.6 Communication Interfacing

The VK0256 communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required ($/CS$, $/WR$, and $DATA$); $/RD$ is optional for reading.

- $/CS$: Chip select input. It enables the serial interface when low and terminates communication when high.
- $/RD$: Read clock input. On the falling edge, data is output from the device onto the $DATA$ line.
- $/WR$: Write clock input. On the rising edge, data and commands from $DATA$ are latched into the device.
- $DATA$: Bidirectional serial data line used to transfer both command and display data.
- $/IRQ$: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

7.7 Command Format

The VK0192 is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: $READ$, $WRITE$, and $READ-MODIFY-WRITE$.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

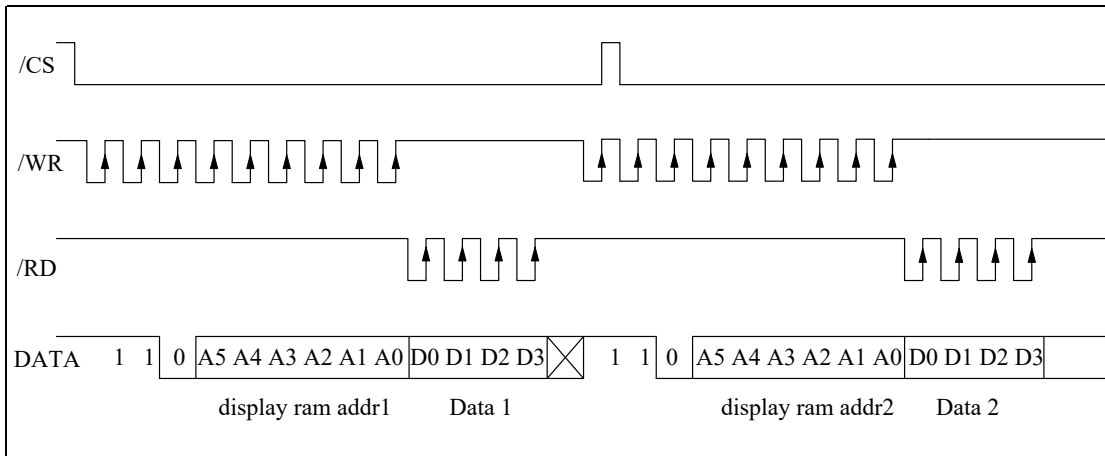
Operation	MODE	ID
$READ$	$DATA$	110
$WRITE$	$DATA$	101
Read-Modify-Write	$DATA$	101
$COMMAND$	$COMMAND$	100

8 CMD/Data Timing Diagrams

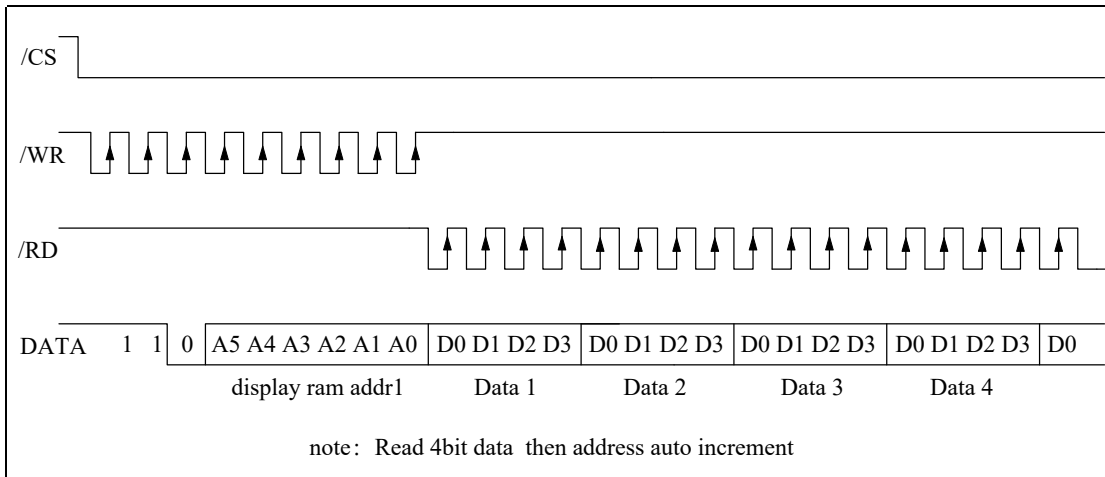
The command sequence corresponds to four ID codes.

8.1 READ Mode

Command code: 110

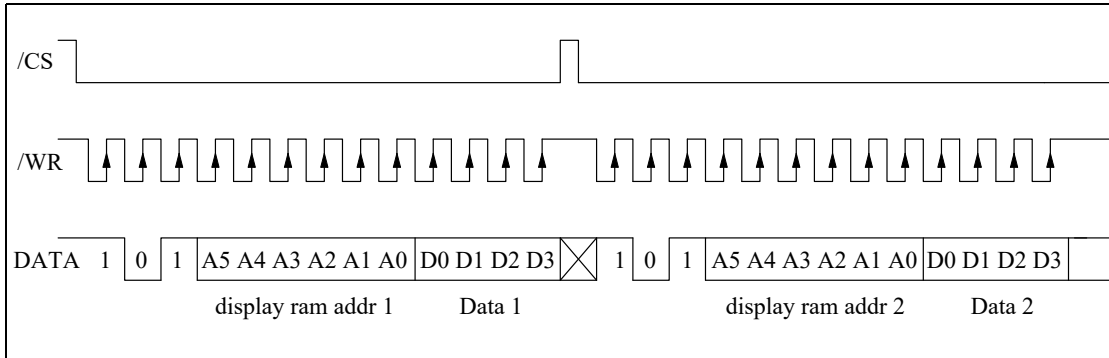


Successive Address Reading

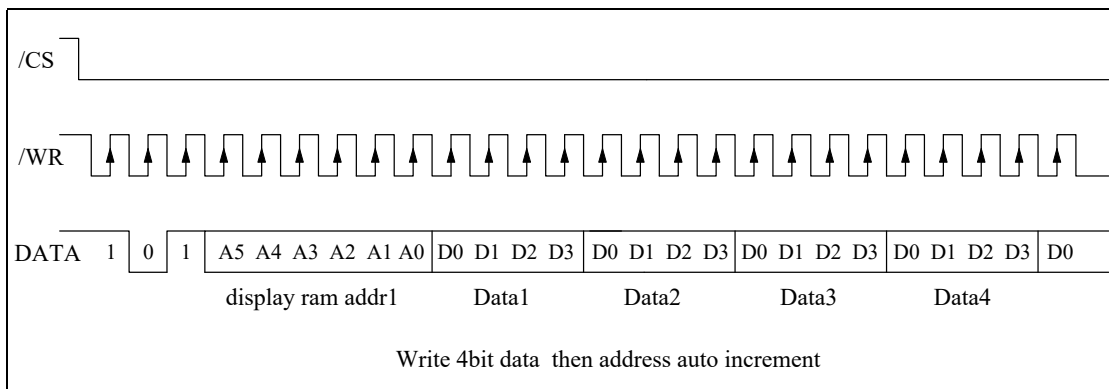


8.2 WRITE Mode

Command code: 101

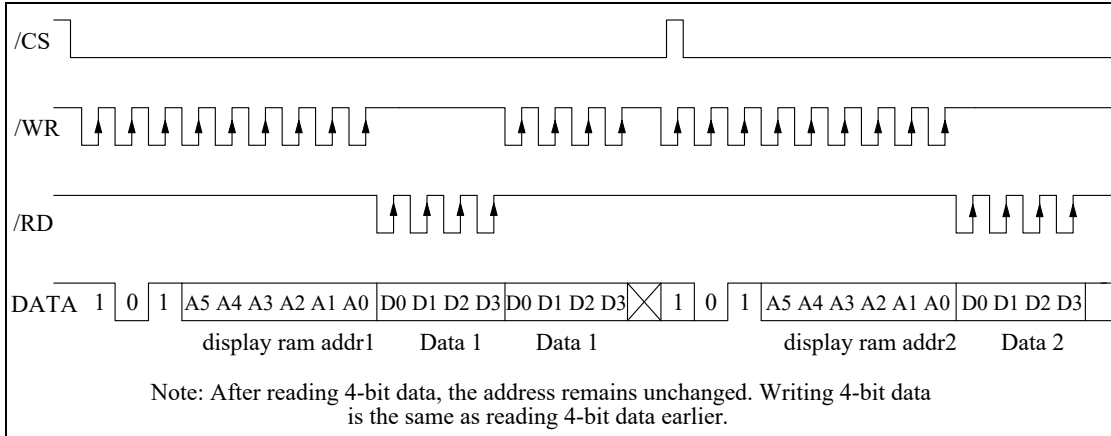


Successive Address Writing

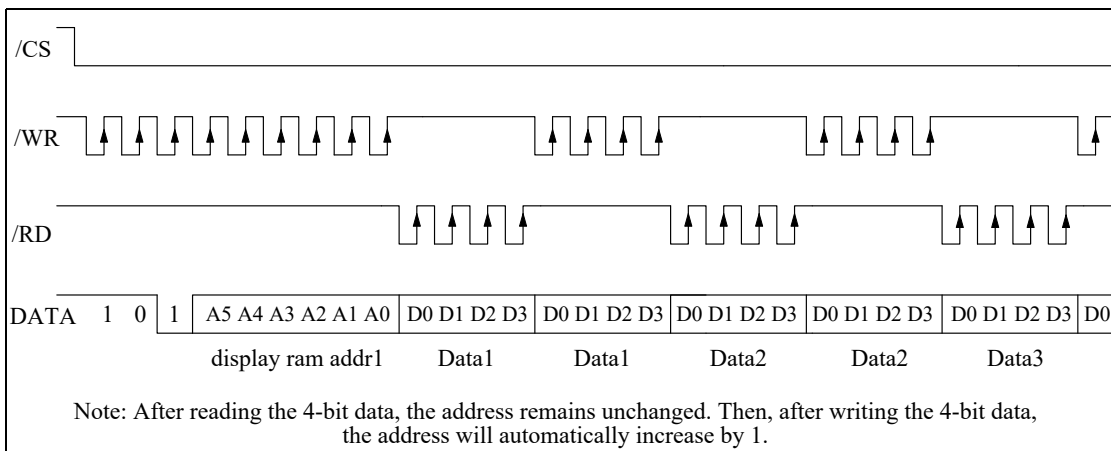


8.3 Read-Modify-Write Mode

Command Code : 101

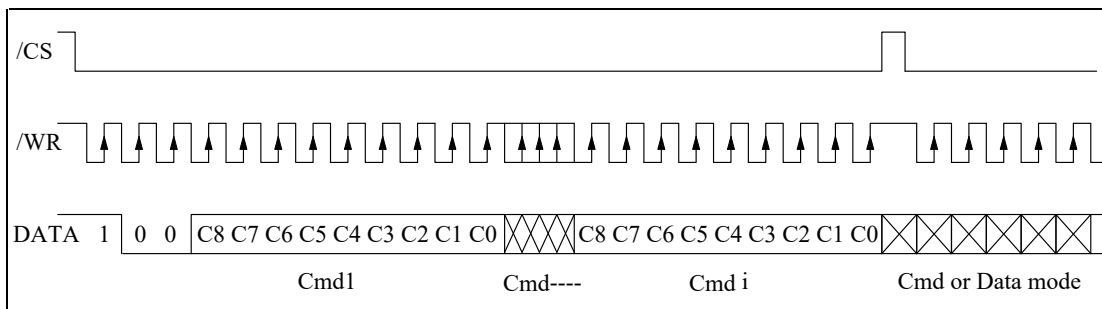


Successive Address Accessing



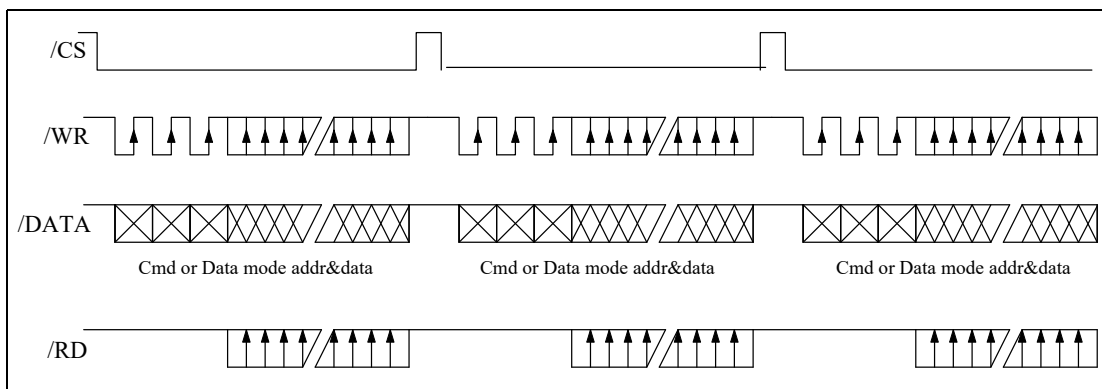
8.4 Command Mode

Command Code : 100



8.5 Data and Command Mode

Data and Command Mode



9 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on the system clock	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC 32k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

Note : X: 0 or 1

D/C:Data/Command mode

A5-A0: Display RAM addresses

Def.:Power on reset default

D3-D0:4bit Display RAM data

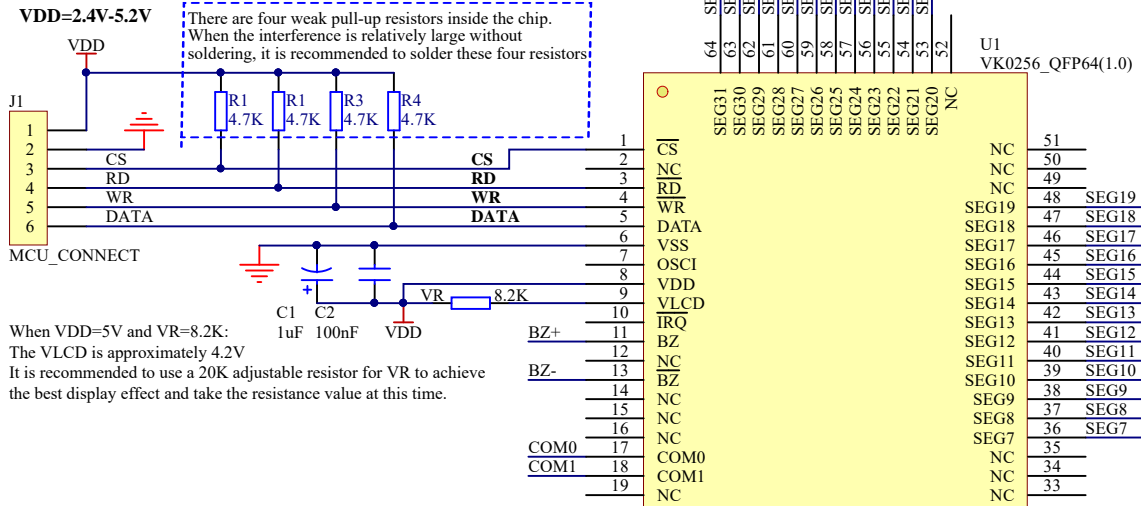
110,101and 100 is Command ID

10 Application Circuits

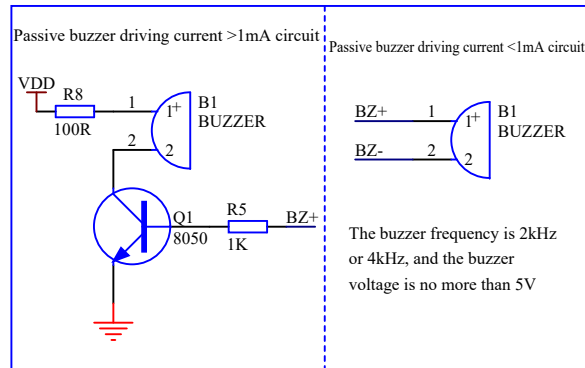
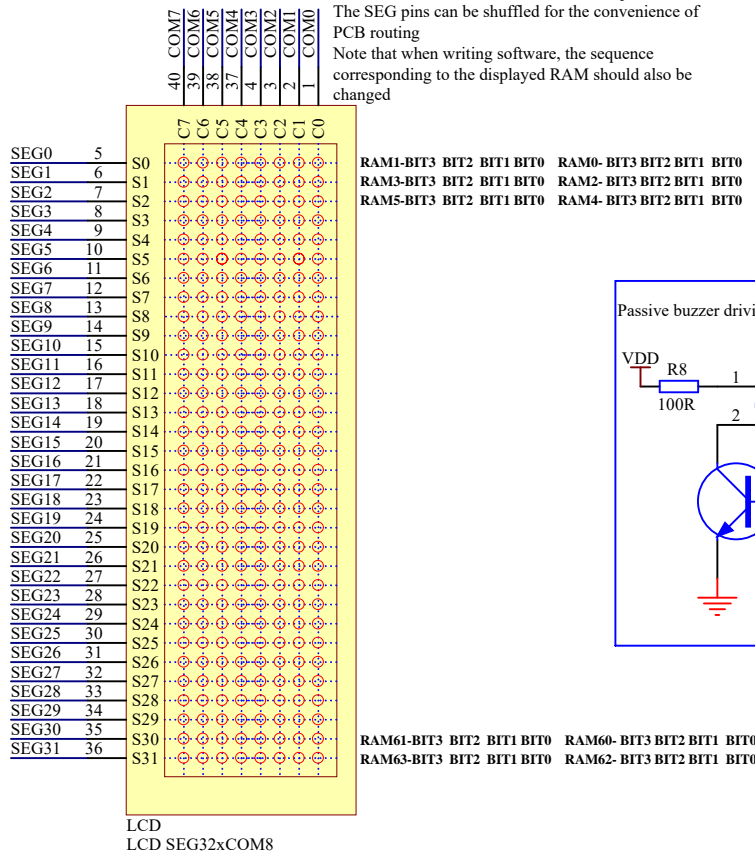
When the LCD only displays, the RD pin can be left floating and not connected

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin

When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed



11 Electrical characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~5.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

11.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	IDD1	—	80	210	μA	3V	No load/LCD ON On-chip RC oscillator
		—	135	415		5V	
Operating current	IDD2	—	8	30	μA	3V	No load/LCD OFF On-chip RC oscillator
		—	20	55		5V	
Standby Current	ISTB	—	1	8	μA	3V	No load, Power down mode
		—	2	16		5V	
Input Low Voltage	VIL	0	—	0.6	V	3V	DATA, /WR, /CS, /RD
		0	—	1.0		5V	
Input High Voltage	VIH	2.4	—	3.0	V	3V	DATA, /WR, /CS, /RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	IOL1	0.9	1.8	—	mA	3V	VOL=0.3V
		1.7	3.0	—		5V	VOL=0.5V
BZ, /BZ	IOH1	-0.9	-1.8	—	mA	3V	VOH=2.7V
		-1.7	-3.0	—		5V	VOH=4.5V
DATA	IOL1	200	450	—	μA	3V	VOL=0.3V
		250	500	—		5V	VOL=0.5V
DATA	IOH1	-200	-450	—	μA	3V	VOH=2.7V
		-250	-500	—		5V	VOH=4.5V
LCD Sink Current	IOL2	15	40	—	μA	3V	VOL=0.3V
		100	200	—		5V	VOL=0.5V
LCD COM Source Current	IOH2	-15	-30	—	μA	3V	VOH=2.7V
		-45	-90	—		5V	VOH=4.5V
LCD SEG Sink Current	IOL3	15	30	—	μA	3V	VOL=0.3V
		70	150	—		5V	VOL=0.5V
LCD SEG Source Current	IOH3	-6	-13	—	μA	3V	VOH=2.7V
		-20	-40	—		5V	VOH=4.5V
Pull-UP Resistor	RUP	100	200	300	kΩ	3V	DATA, /WR, /CS, /RD
		50	100	150		5V	

11.3 AC Electrical Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	22	32	40	kHz	3V	On-chip RC oscillator
		24	32	40		5V	
System Clock	f_{SYS2}	—	32	—	kHz	3V	External clock source
		—	32	—		5V	
LCD Clock	f_{LCD1}	44	64	80	Hz	3V	On-chip RC oscillator
		48	64	80		5V	
	f_{LCD2}	—	64	—	Hz	3V	External clock source
		—	64	—		5V	
LCD Common Period	t_{COM}	—	n/f_{LCD}	—	sec	—	N: Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

Figure 1

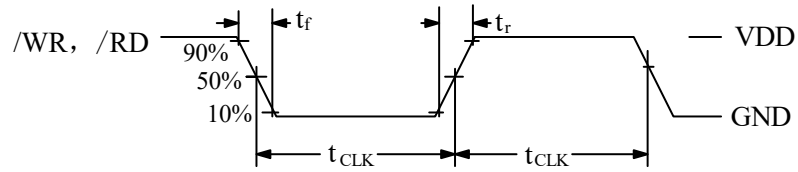


Figure 2

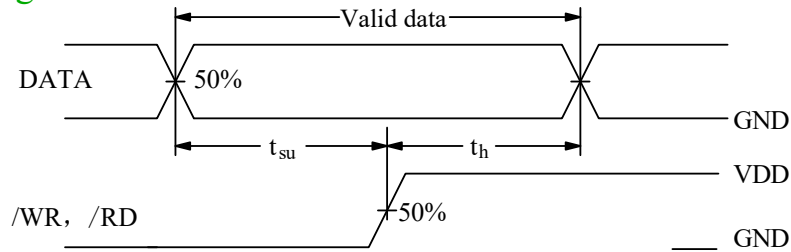


Figure 3

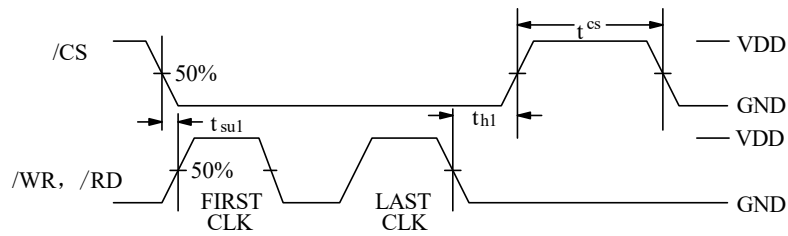
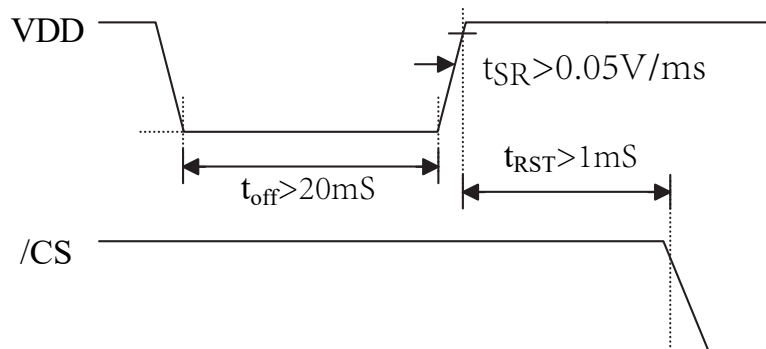
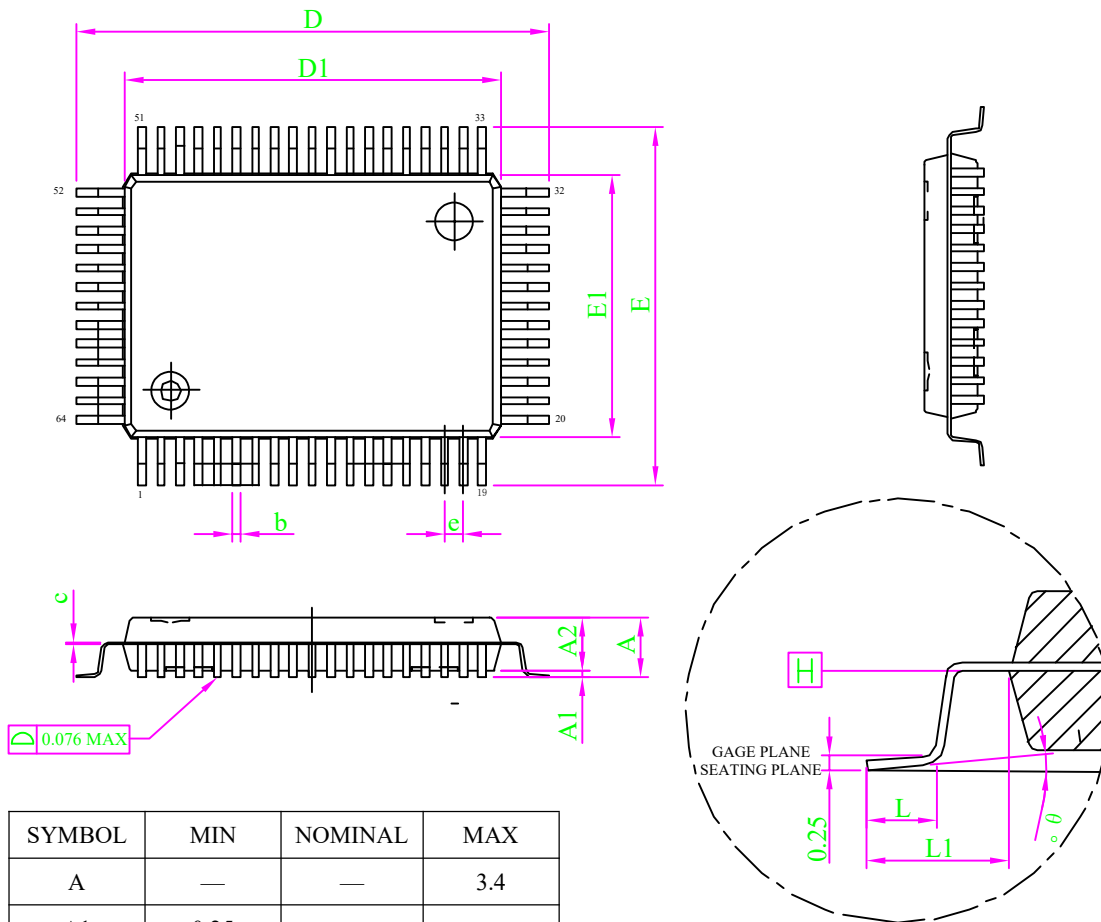


Figure 4



12 Package Information

12.1 QFP64(20.0mm x 14.0mm PP=1.0mm)



SYMBOL	MIN	NOMINAL	MAX
A	—	—	3.4
A1	0.25	—	—
A2	2.55	2.72	3.05
b	0.35	0.40	0.50
c	0.11	0.15	0.23
D	25.00 BASIC		
D1	20.00 BASIC		
e	1.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
L	1.15	1.30	1.45
L1	2.50REF		
θ°	0	3.5	7

UNIT: mm

NOTES:

- 1.JEDEC:N/A
- 2.DATUM PLANE \square IS LOCATED AT THE BOTTOM OF THE MOLO PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- 3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE \square .
- 4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

13 Disclaimer

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14 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Check alignment	YES
4	1.3	2025-05-13	Update version	YES

[1] Consult the recently published documents before starting or finishing the design.

[2] Since the release of this document , the device product status described in this document may have changed and may differ in several cases. The latest product status information can be found on the Internet at <https://www.szvinka.com/>