

Features

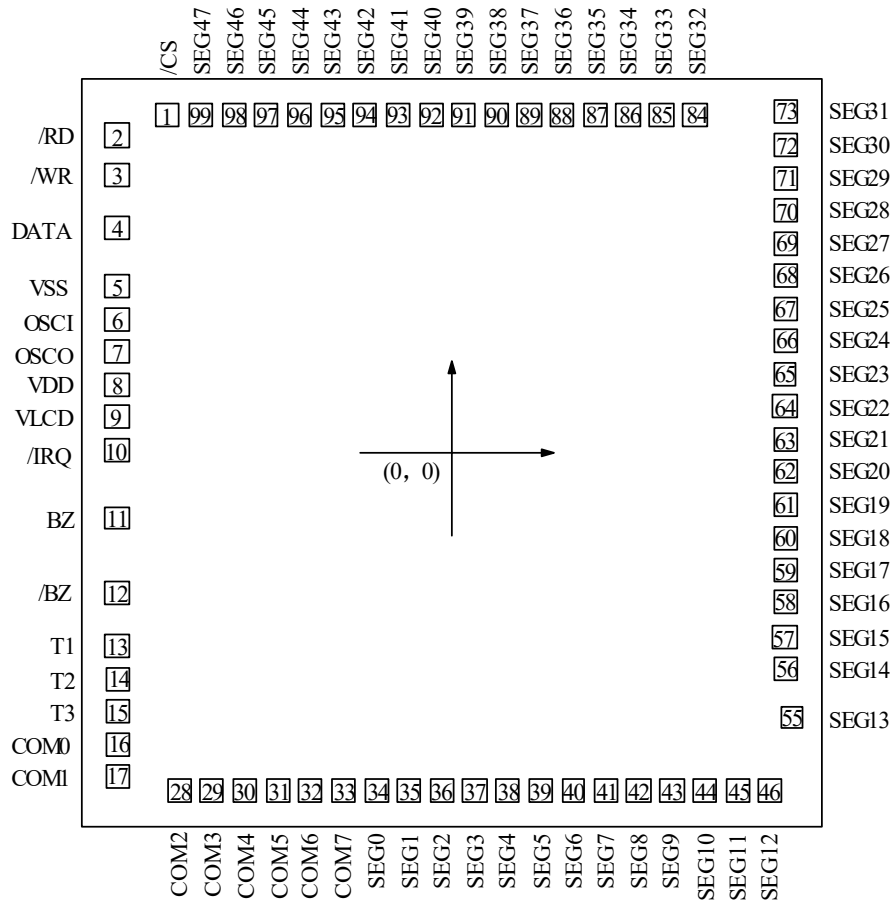
- Operating voltage:2.4-5.2V
- Built-in 32kHz RC oscillator (default)
- External 32.768kHz crystal (OSCO,OSCI)
- 1/4 BIAS
- 1/8 duty (8 COM)
- Built-in 48×8 bit display RAM
- Selection of buzzer frequencies 2kHz、4kHz
- STANDBY mode (by Cmd LCD OFF,SYS DIS)
- 8 kinds of time base/WDT clock sources
- Time base or WDT overflow output (/IRQ pin)
- 3 or 4 wire serial interface
- Software configuration LCD parameters
- Data mode and command mode instructions
- Read/Write address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage (<VDD)
- Package:
 - LQFP100(14.0mm x 14.0mm PP=0.5mm)
 - QFP100(20.0mm x 14.0mm PP=0.65mm)
 - DICE
 - COG

1 General Description

VK1623S is a RAM Mapping 48x8 LCD Driver , It can support LCD screens with a maximum of 384 pattern(48SEGx8COM).Only 3 or 4 lines are required to communication interface with the VK1623S,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command (by Cmd LCD OFF,SYS DIS) .

2 COB PAD description and Coordinates

2.1 COB PAD Assignment



Chip size: 2730 × 2730 um²

Substrate: connected to VDD

PAD size: 90 × 90 um

PAD spacing: 112 um note: VLCD < VDD

2.2 COB PAD Coordinates

coordinate origin is in the center of the chip, unit: μm

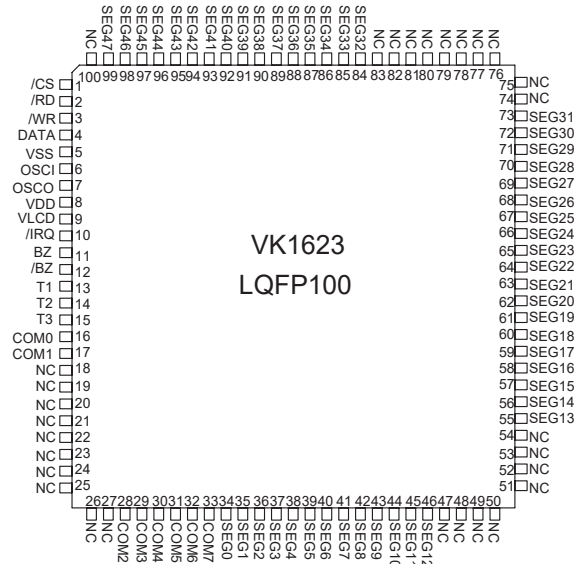
Pad No	Name	X	Y	Pad No	Name	X	Y
1	/CS	-1076	1288	51	NC	—	—
2	/RD	-1270	1212	52	NC	—	—
3	/WR	-1270	1062	53	NC	—	—
4	DATA	-1270	860	54	NC	—	—
5	VSS	-1270	638	55	SEG13	1293	-1008
6	OSCI	-1270	513	56	SEG14	1270	-823
7	OSCO	-1270	388	57	SEG15	1270	-698
8	VDD	-1270	263	58	SEG16	1270	-573
9	VLCD	-1270	138	59	SEG17	1270	-448
10	/IRQ	-1270	13	60	SEG18	1270	-323
11	BZ	-1270	-249	61	SEG19	1270	-198
12	/BZ	-1270	-534	62	SEG20	1270	-73
13	T1	-1270	-738	63	SEG21	1270	51
14	T2	-1270	-863	64	SEG22	1270	176
15	T3	-1270	-988	65	SEG23	1270	301
16	COM0	-1270	-1113	66	SEG24	1270	426
17	COM1	-1270	-1238	67	SEG25	1270	551
18	NC	—	—	68	SEG26	1270	676
19	NC	—	—	69	SEG27	1270	801
20	NC	—	—	70	SEG28	1270	926
21	NC	—	—	71	SEG29	1270	1051
22	NC	—	—	72	SEG30	1270	1176
23	NC	—	—	73	SEG31	1270	1301
24	NC	—	—	74	NC	—	—
25	NC	—	—	75	NC	—	—
26	NC	—	—	76	NC	—	—
27	NC	—	—	77	NC	—	—

coordinate origin is in the center of the chip, unit: μm

Pad No	Name	X	Y	Pad No	Name	X	Y
28	COM2	-1035	-1288	78	NC	—	—
29	COM3	-910	-1288	79	NC	—	—
30	COM4	-785	-1288	80	NC	—	—
31	COM5	-660	-1288	81	NC	—	—
32	COM6	-535	-1288	82	NC	—	—
33	COM7	-410	-1288	83	NC	—	—
34	SEG0	-285	-1288	84	SEG32	923	1289
35	SEG1	-160	-1288	85	SEG33	798	1289
36	SEG2	-35	-1288	86	SEG34	673	1289
37	SEG3	90	-1288	87	SEG35	548	1289
38	SEG4	215	-1288	88	SEG36	423	1289
39	SEG5	340	-1288	89	SEG37	298	1289
40	SEG6	465	-1288	90	SEG38	173	1289
41	SEG7	590	-1288	91	SEG39	48	1289
42	SEG8	715	-1288	92	SEG40	-76	1289
43	SEG9	840	-1288	93	SEG41	-201	1289
44	SEG10	965	-1288	94	SEG42	-326	1289
45	SEG11	1090	-1288	95	SEG43	-451	1289
46	SEG12	1215	-1288	96	SEG44	-576	1289
47	NC	—	—	97	SEG45	-701	1289
48	NC	—	—	93	SEG46	-826	1289
49	NC	—	—	99	SEG47	-951	1289
50	NC	—	—	100	NC	—	—

3.1 Pinouts and pin description

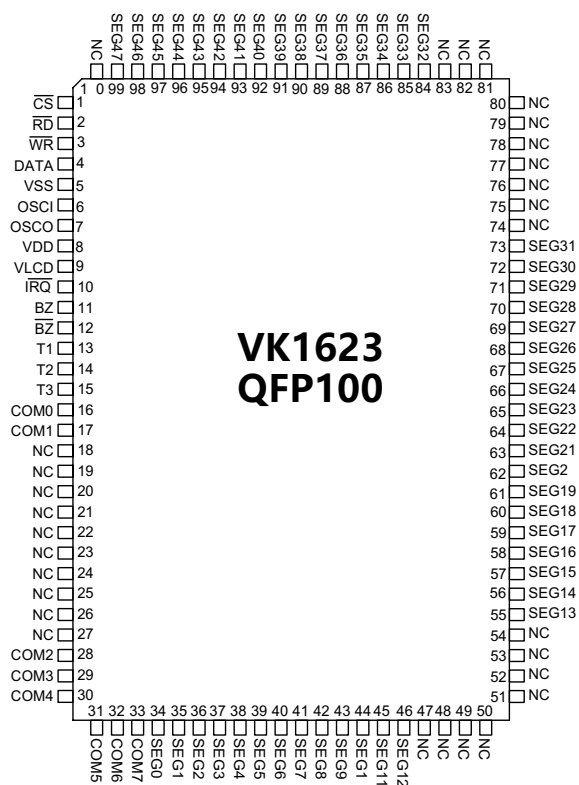
3.1 VK1623S LQFP100 Pin Assignment



3.2 VK1623 LQFP100 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip selection input with pull-up resistor 1-disable, 0-enable.
2	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD power input
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair, when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-15	T1-T3	—	---
16,17 28-33	COM0-COM7	O	LCD COM outputs
34-46 55-73 84-99	SEG0-SEG47	O	LCD SEG outputs

3.3VK1623S QFP100 Pin Assignment

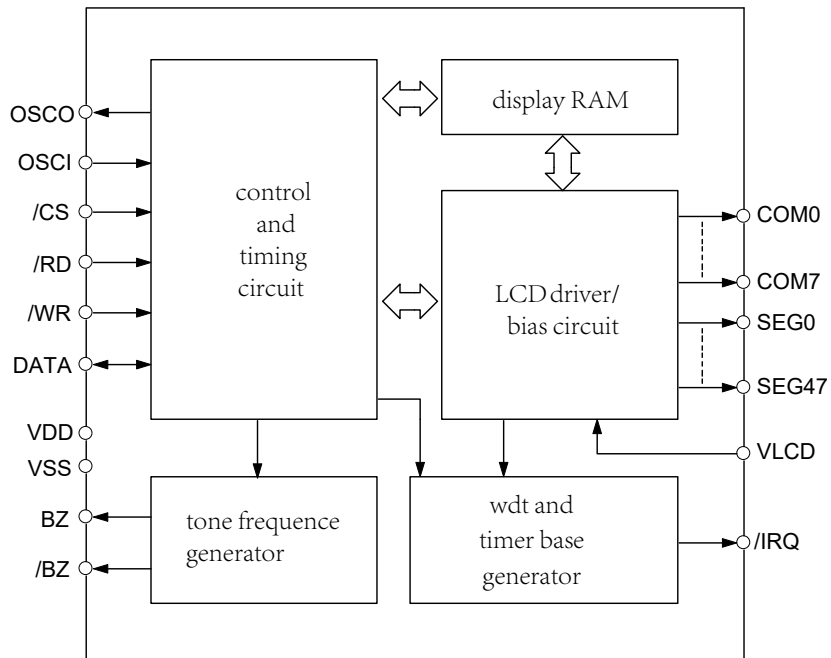


3.4 VK1623S QFP100 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip selection input with pull-up resistor 1-disable, 0-enable.
2	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD power input
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair , when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-15	T1-T3	—	---
16,17 28-33	COM0-COM7	O	LCD COM outputs
34-46 55-73 84-99	SEG0-SEG47	O	LCD SEG outputs

4 Functional Description

4.1 Block diagram



4.2 Display RAM

The static display memory (RAM) is organized into 48×8 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands.

The following is a mapping from the RAM to the LCD pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0		
SEG0					1					0	address 7 bit (A6---A0)
SEG1					3					2	
SEG2					5					4	
SEG3					7					6	
⋮					⋮					⋮	
SEG47					95					94	
	D3	D2	D1	D0	Data\Addr	D3	D2	D1	D0	Data\Addr	

4.3 Time Base and WDT

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT) is composed of an 8-stage time base generator along with a 2-stage count-up counter, it is designed to break the host controller from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the /IRQ pin by a command option. There are totally 8 frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

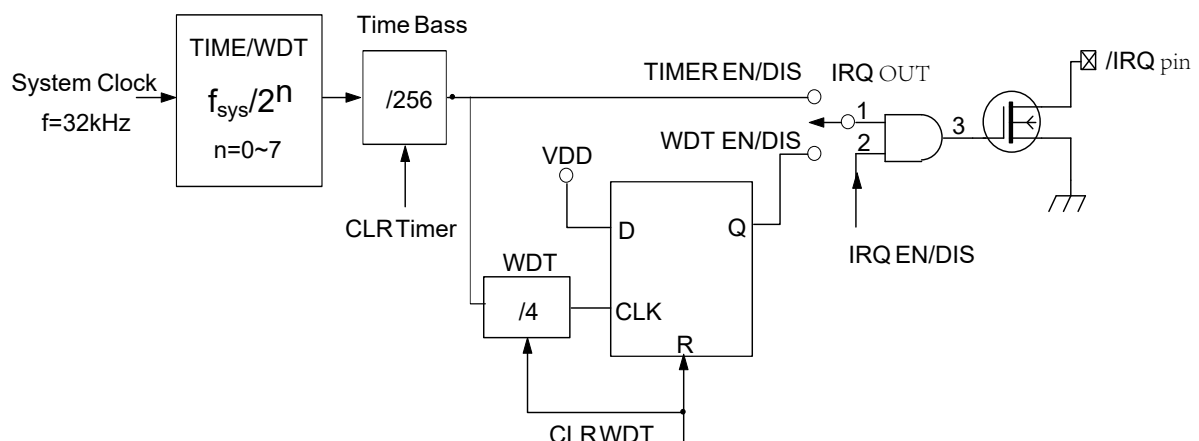
$$f_{WDT} = f_{sys} / 2^n \quad (n=0 \sim 7) \quad f_{sys} = 32\text{kHz}$$

The time base generator and WDT share the same 8-stage counter. WDT is cleared by executing the CLR WDT command, time base generator is cleared by executing the CLR WDT or the CLR TIMER command.

Executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the /IRQ pin). invoking the WDT DIS command disables the time base generator. After the TIMER EN command is transferred, the WDT is disconnected from the /IRQ pin, and the output of the time base generator is connected to the /IRQ pin.

The /IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command. After the system power on, the /IRQ will be disabled.

Timer and WDT Configurations:



4.4 Tone Output

VK1623S has a simple 2KHz / 4kHz tone generator , it can output a pair of differential driving signals on the BZ and /BZ, which are used to generate a single tone .By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable .The tone output can be turned on or off by invoking the TONE 4k/TONE 2k or the TONE OFF command. The tone outputs, namely BZ and /BZ, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the /BZ outputs will remain at low level.

4.5 LCD Driver

The VK1623S is a 384 (48×8) pattern LCD driver, 1/4bias and 1/8duty (8 com).

4.5.1 Communication Interfacing

Four lines are required to interface with the VK1623S. If only used for display, only 3 pins can be used.

The /CS pin is used to initialize the serial interface circuit and to terminate the communication with HOST.

The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The /RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the /RD signal, and the clocked out data will then appear on the DATA line.

The /WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the VK1623S on the rising edge of the WR signal.

The /IRQ pin can be selected as a timer output or a WDT overflow flag output by the software setting, it is a NMOS open drain output.

4.5.2 Command Format

VK1623S can be configured by the Software setting. There are two mode commands to configure the LCD parameters and to transfer the LCD display data. The configuration mode of the VK1623S is called command mode, and its command mode ID is 1 0 0. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode IDs and the command mode ID:

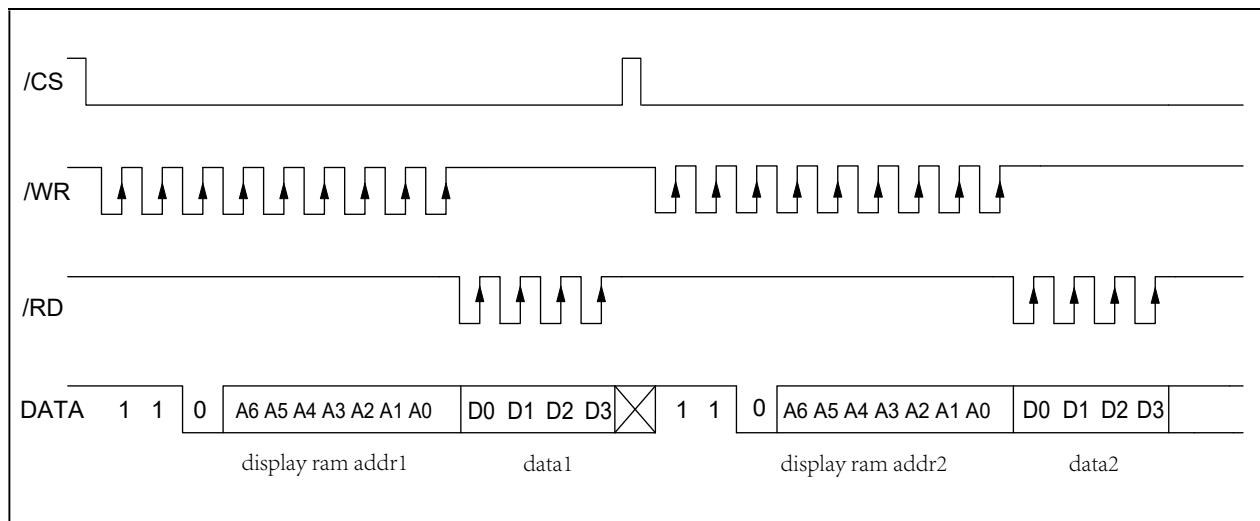
Operation	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

4.5.3 Cmd/Data Timing Diagrams

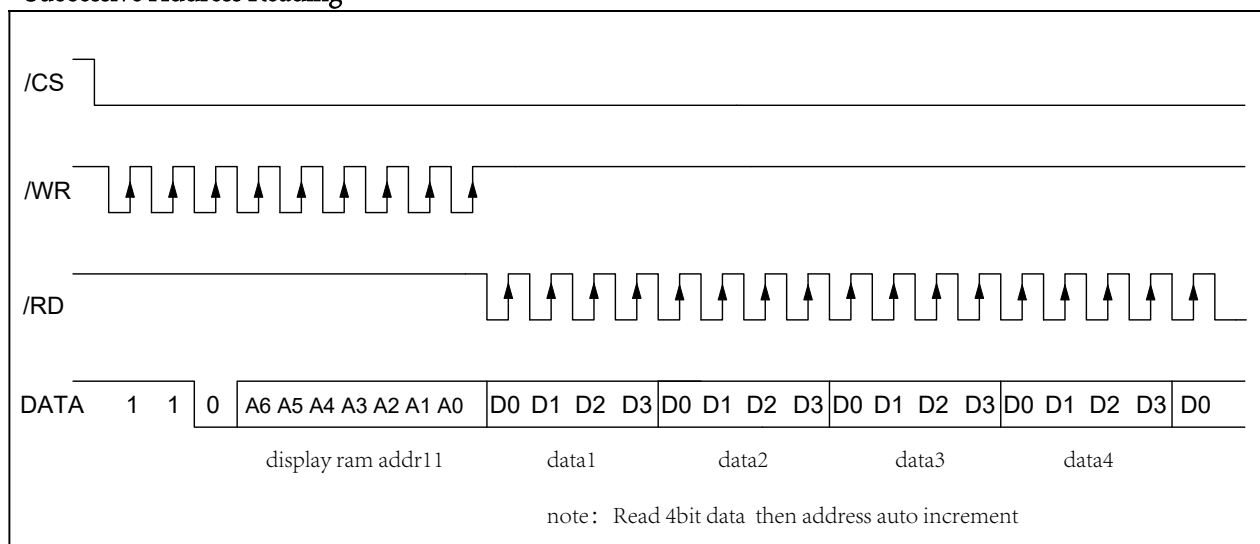
The following are the data mode IDs and the command mode ID Timing Diagrams.

4.5.3.1 READ Mode

Command Code : 110

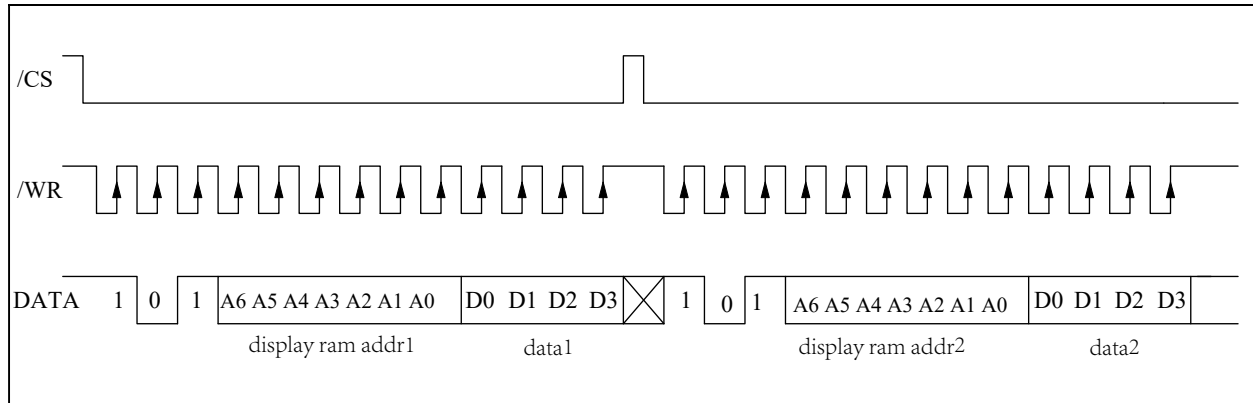


Successive Address Reading

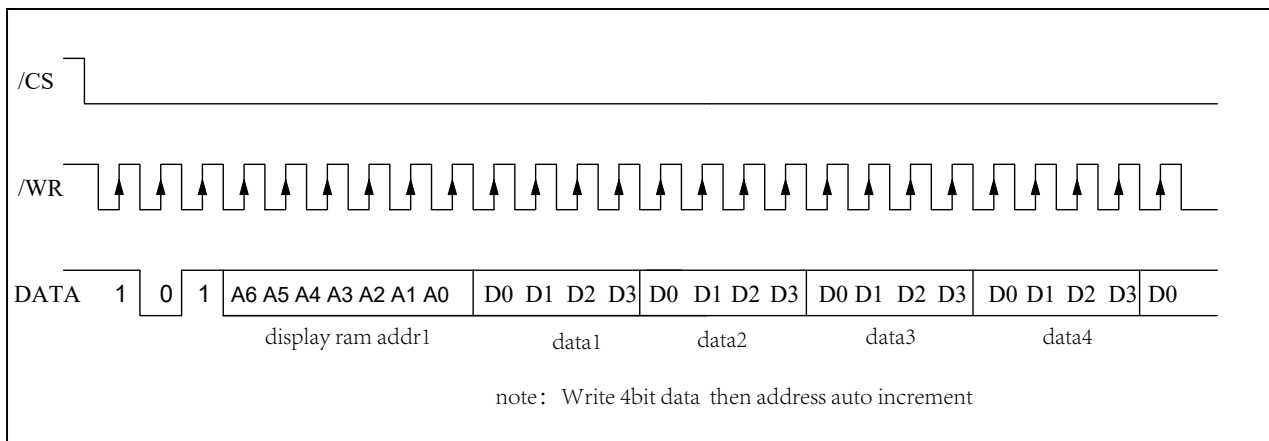


4.5.3.2 WRITE Mode

Command Code : 101

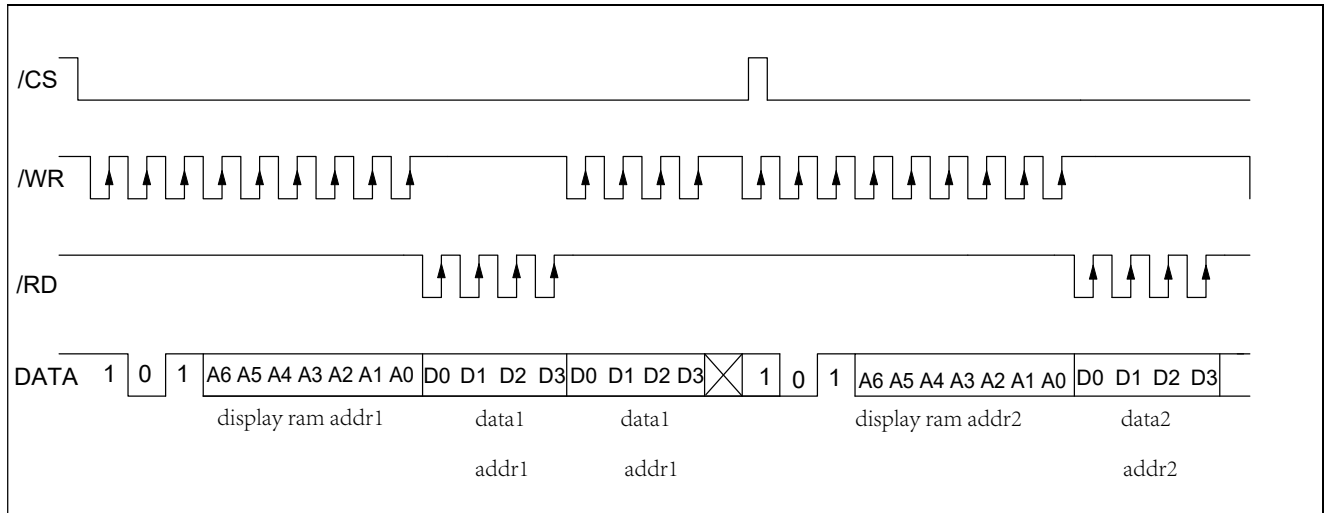


Successive Address Writing

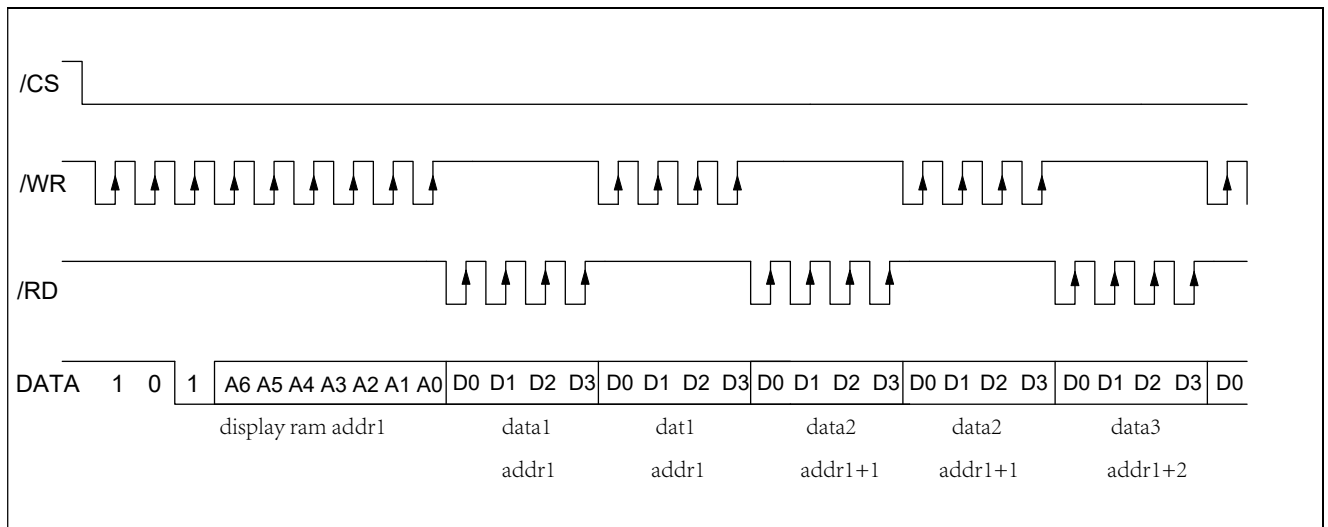


4.5.3.3 Read-Modify-Write Mode

Command Code : 101

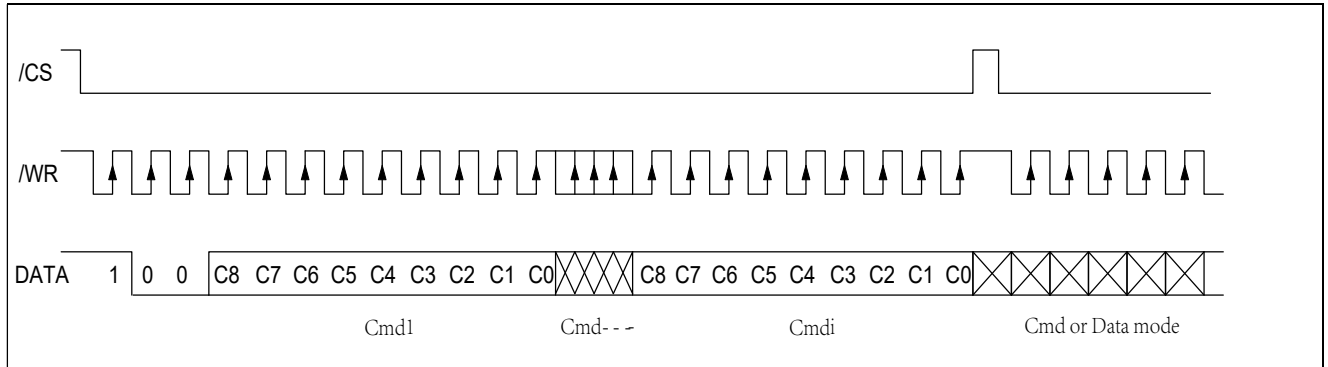


Successive Address Accessing



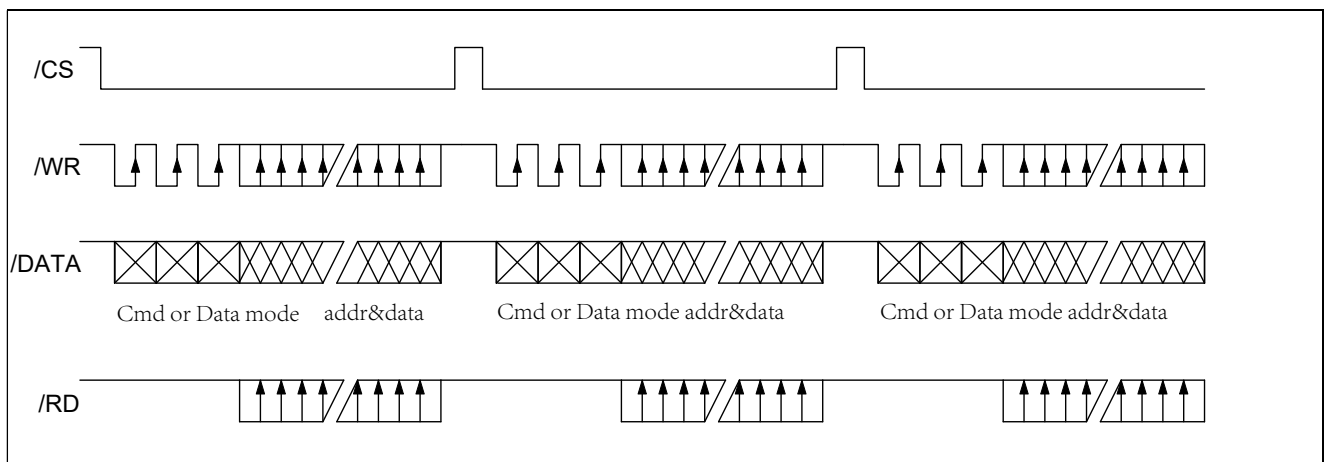
4.5.3.4 Command Mode

Command Code : 100



4.5.3.5 Data and Command Mode

Data and Command Mode



5 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000- 0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000- 0001-X	C	Turn on system oscillator	
LCD OFF	100	0000- 0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000- 0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000- 0100-X	C	Disable time base output	
WDT DIS	100	0000- 0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000- 0110-X	C	Enable time base output	
WDT EN	100	0000- 0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000- 1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC 32k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

note.: X: 0 or 1

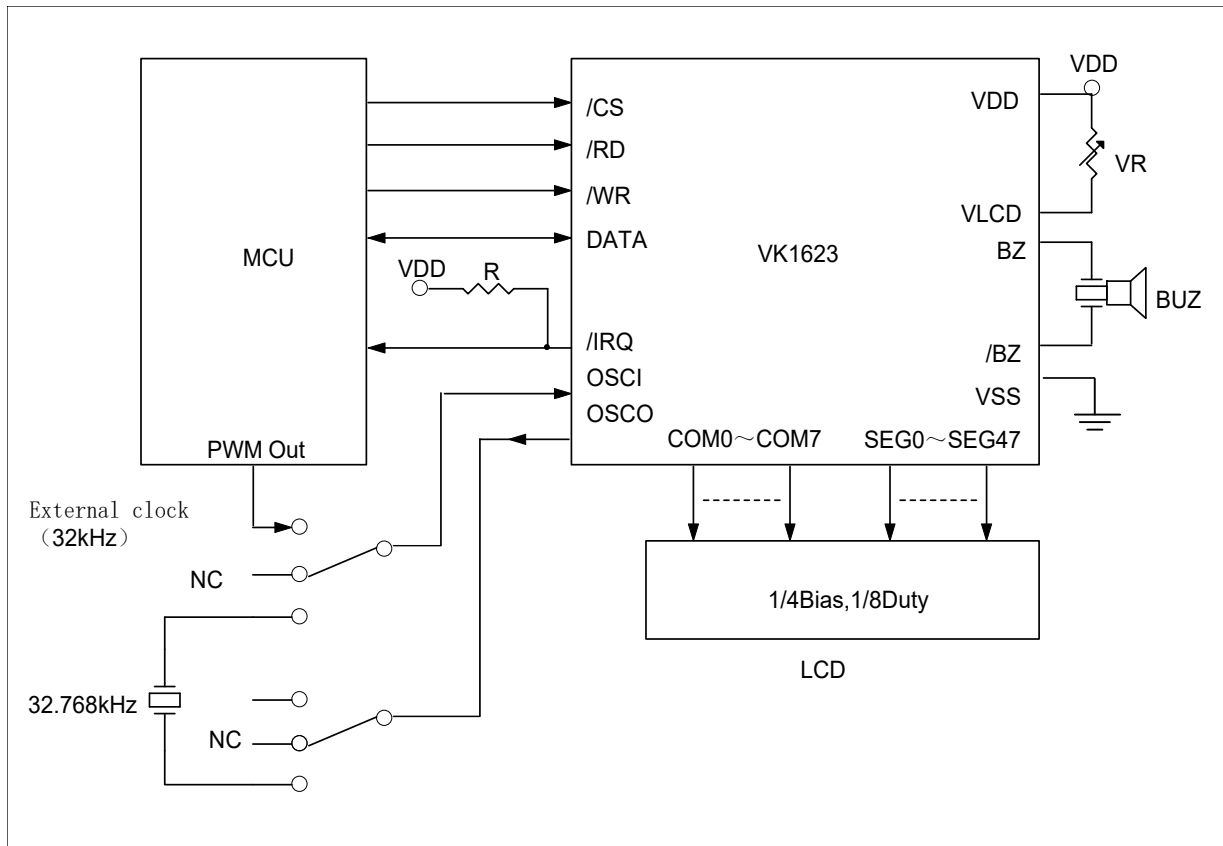
A6-A0: Display RAM addresses
D3-D0:4bit Display RAM data

D/C:Data/Command mode

Def.:Power on reset default

110,101 and 100 is Command ID

6 Application Circuits



Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

7 Electrical characteristics

7.1 Absolute Maximum Ratings

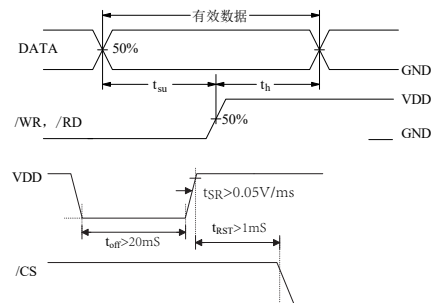
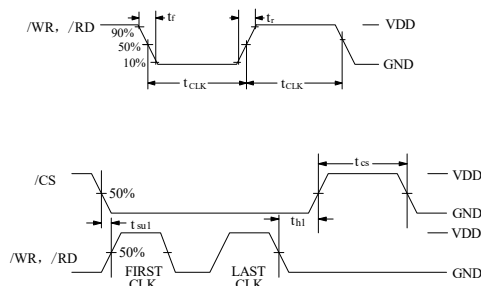
Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3~5.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

7.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I _{DD1}	—	155	310	μA	3V	No load/LCD ON
		—	260	420		5V	On-chip RC oscillator
Operating current	I _{DD2}	—	150	310	μA	3V	No load/LCD ON
		—	250	420		5V	External crystal
Operating current	I _{DD11}	—	8	30	μA	3V	No load/LCD OFF
		—	20	60		5V	On-chip RC oscillator
Operating current	I _{DD22}	—	—	20	μA	3V	No load/LCD OFF
		—	—	35		5V	External crystal
Standby Current	I _{STB}	—	1	10	μA	3V	No load,
		—	2	20		5V	Power down mode
Input Low Voltage	V _{IL}	0	—	0.6	V	3V	DATA, /WR, /CS, /RD
		0	—	1.0		5V	
Input High Voltage	V _{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS, /RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	I _{OL1}	0.9	1.8	—	mA	3V	V _{OL} =0.3V
		1.7	3.0	—		5V	V _{OL} =0.5V
BZ, /BZ	I _{OH1}	-0.9	-1.8	—	mA	3V	V _{OH} =2.7V
		-1.7	-3.0	—		5V	V _{OH} =4.5V
DATA	I _{OL1}	0.9	1.8	—	mA	3V	V _{OL} =0.3V
		1.7	3.0	—		5V	V _{OL} =0.5V
DATA	I _{OH1}	-0.9	-1.8	—	mA	3V	V _{OH} =2.7V
		-1.7	-3.0	—		5V	V _{OH} =4.5V
LCD COM Sink Current	I _{OL2}	80	160	—	μA	3V	V _{OL} =0.3V
		180	360	—		5V	V _{OL} =0.5V
LCD COM Source Current	I _{OH2}	-40	-80	—	μA	3V	V _{OH} =2.7V
		-90	-180	—		5V	V _{OH} =4.5V
LCD SEG Sink Current	I _{OL3}	50	100	—	μA	3V	V _{OL} =0.3V
		120	240	—		5V	V _{OL} =0.5V
LCD SEG Source Current	I _{OH3}	-30	-60	—	μA	3V	V _{OH} =2.7V
		-70	-140	—		5V	V _{OH} =4.5V
Pull-UP Resistor	R _{UP}	100	200	300	kΩ	3V	DATA, /WR, /CS, /RD
		50	100	150		5V	

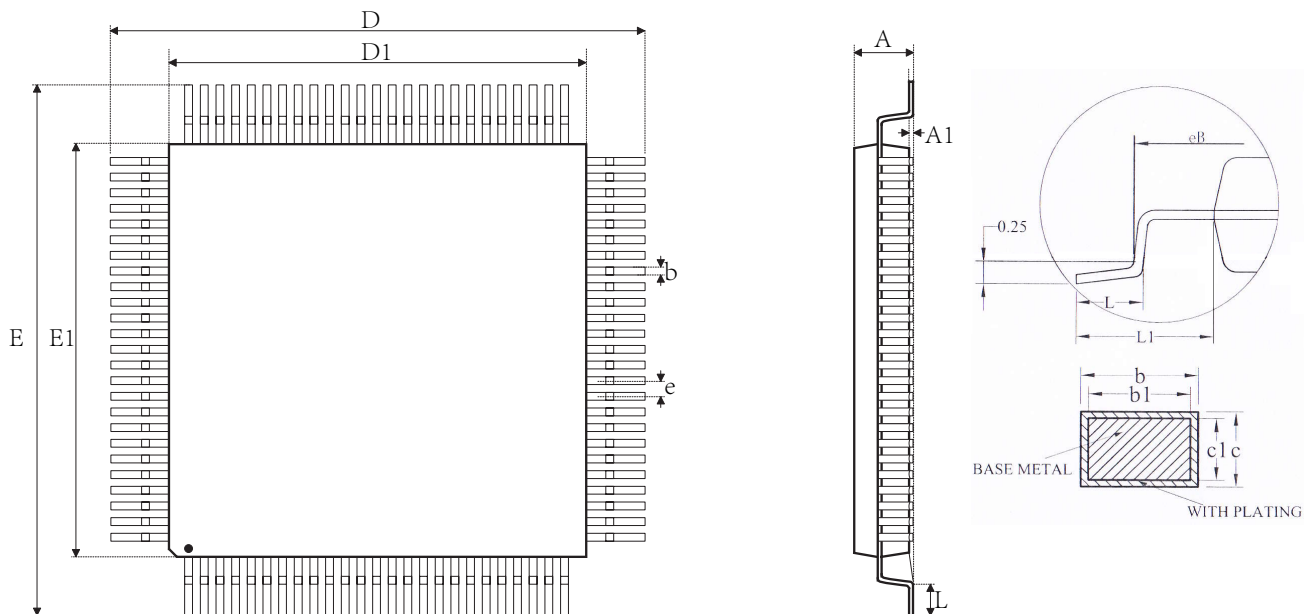
7.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f _{SYS1}	22	32	40	kHz	3V	On-chip RC oscillator
		24	32	40		5V	
System Clock	f _{SYS2}	—	32	—	kHz	3V	External clock source
		—	32	—		5V	
LCD Clock	f _{LCD1}	44	64	80	Hz	3V	On-chip RC oscillator
		48	64	80	Hz	5V	
	f _{LCD2}	—	64	—	Hz	3V	External clock source
		—	64	—	Hz	5V	
LCD Common Period	t _{COM}	—	N/ f _{LCD}	—	sec	—	N: Number of COM
Serial Data Clock (/WR)	F _{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock (/RD)	F _{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t _{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t _{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
	t _{CLK}	1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t _r , t _f	—	120	—	ns	3V	—
		—	120	—		5V	
Setup Time for DATA to /WR, /RD Clock Width	t _{su}	—	120	—	ns	3V	—
		—	120	—		5V	
Hold Time for DATA to /WR, /RD Clock Width	t _h	—	120	—	ns	3V	—
		—	120	—		5V	
Setup Time for /CS to /WR, /RD Clock Width	t _{su1}	—	100	—	ns	3V	—
		—	100	—		5V	
Hold Time for /CS to /WR, /RD Clock Width	t _{h1}	—	100	—	ns	3V	—
		—	100	—		5V	



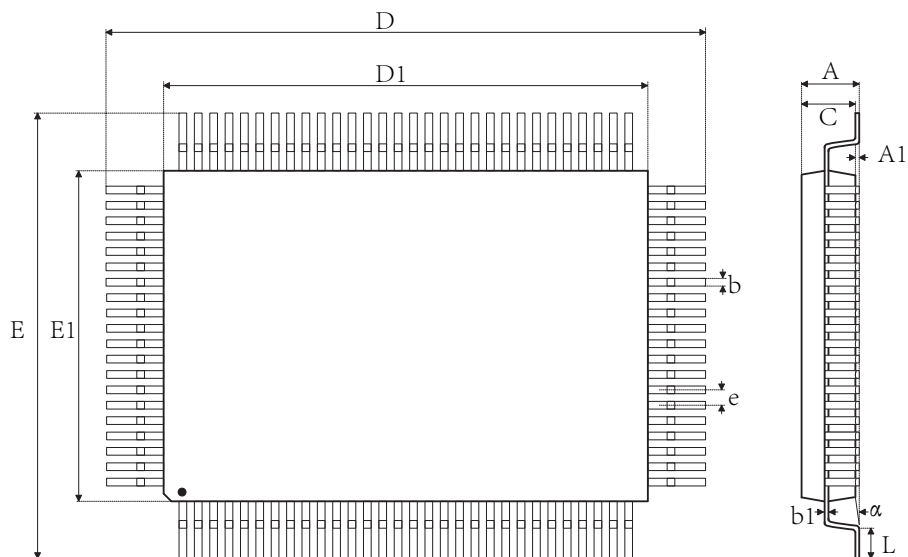
8.1 Package Information

8.1 LQFP100(14.0mmx14.0mm PP=0.5mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		

8.2 QFP100(20.0mm×14.0mm PP=0.65mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	3.40
A1	0.25	--	0.50
b	--	0.3	--
b1	0.10	--	0.20
C	2.57	2.72	2.87
D	23.65	23.90	24.15
D1	19.90	20.00	20.10
E	17.65	17.90	18.15
E1	13.90	14.00	14.10
α	0°	--	7°
e	0.65BSC		
L	0.65	0.80	0.95

9 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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