



VK2C21A DATA BOOK

20×4/16×8 LCD DRIVER

Rev.1.3

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1 General Description

The VK2C21A is a dot-matrix store-mapped LCD driver that supports LCD screens with a maximum of 80 dots (20SEG×4COM) or 128 dots (16SEG×8COM). The single-chip microcomputer can configure display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as industrial control instrument products.

2 Features

- Operating voltage: 2.4-5.5V
- Built-in 32kHz RC oscillator
- Selection of 1/3 or 1/4 bias
- Selection of 1/4 or 1/8 duty
- Built-in 20×4、16×8 bit display RAM
- Selection of 80Hz or 160Hz Frame Frequency
- STANDBY mode (by System Set Command LCD OFF,SYS oscillator OFF)
- I2C bus interface
- Display mode 20×4、16×8
- Three display of the overall flickering frequency
- Software configuration LCD parameters
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage ($\leq VDD$)
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Power-On Reset(POR)
- Low power consumption、High anti-interference
- Package:
SOP28 (300mil) (18.0mm × 7.5mm PP=1.27mm)
DICE
COG

3 Selection List

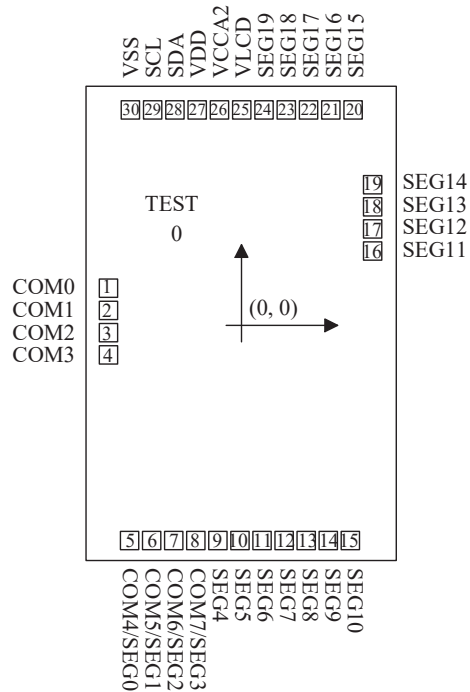
Product name	SEG × COM	BIAS	DUTY	Packaging
VK2C21A	20×4,16×8	1/3,1/4	1/4,1/8	SOP28
VK2C21AA	20×4,16×8	1/3,1/4	1/4,1/8	SSOP28
VK2C21AQ	20×4,16×8	1/3,1/4	1/4,1/8	QFN28L
VK2C21B	16×4,12×8	1/3,1/4	1/4,1/8	SOP24
VK2C21BA	16×4,12×8	1/3,1/4	1/4,1/8	SSOP24
VK2C21BQ	16×4,12×8	1/3,1/4	1/4,1/8	QFN24L
VK2C21C	12×4,8×8	1/3,1/4	1/4,1/8	SOP20
VK2C21CQ	12×4,8×8	1/3,1/4	1/4,1/8	QFN20L
VK2C21D	8×4,4×8	1/3,1/4	1/4,1/8	SOP16
VK2C21DQ	8×4,4×8	1/3,1/4	1/4,1/8	QFN16L

4 Ordering Options

Product name	Packaging	Tube	Plates(volume)	Boxes	PCS	Remark
VK2C21A	SOP28	1 Tube/26		1 Box/2080	20800 PCS	
VK2C21AA	SSOP28	1 Tube/50		1 Box/5000	50000 PCS	
VK2C21AQ	QFN28L		1 volume/490	1 Box/4900	29400 PCS	Braid
VK2C21B	SOP24	1 Tube/30		1 Box/2400	24000 PCS	
VK2C21BA	SSOP24	1 Tube/50		1 Box/10000	100000 PCS	
VK2C21BQ	QFN24L		1 volume/490	1 Box/4900	29400 PCS	Braid
VK2C21C	SOP20	1 Tube/36		1 Box/2880	28800 PCS	
VK2C21CQ	QFN20L		1 volume/490	1 Box/4900	29400 PCS	Braid
VK2C21D	SOP16	1 Tube/50		1 Box/10000	100000 PCS	
VK2C21DQ	QFN16L		1 volume/3000	1 Box/3000	120000 PCS	Braid

5 COB PAD description and Coordinates

5.1 COB PAD Assignment



Chip size: 1150×1715 um², substrate potential: VSS

PAD size: 70×70 um

VDD (Pad27) and VCCA2 (Pad26) must be bound together.

The VLCD (Pad25) and SEG19 (Pad24) must be bound together.

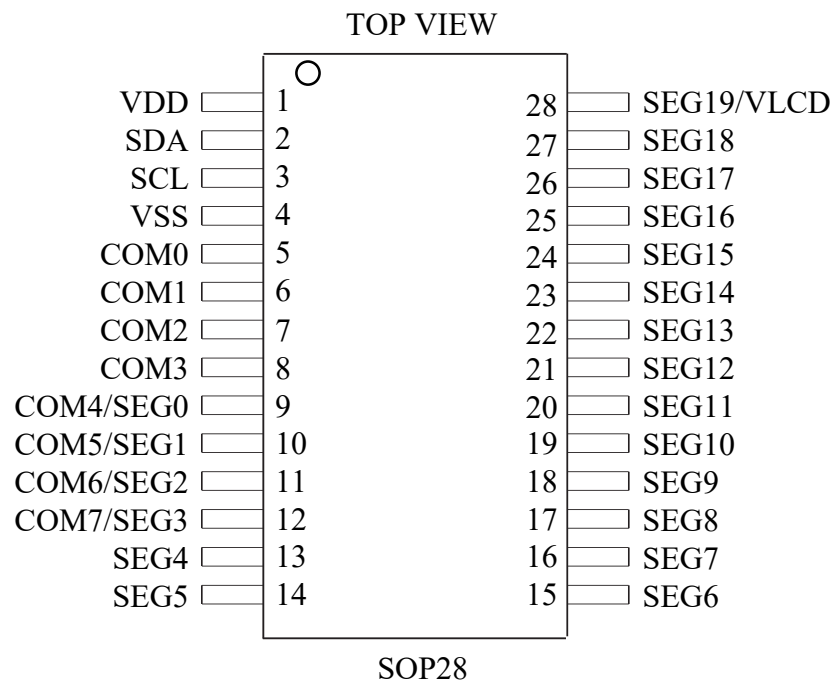
When the VLCD pins are configured to detect the internal bias voltage, the LCD drive voltage can be externally temperature-compensated through the voltage provided by the VLCD pins.

5.2 COB PAD Coordinates

Coordinate origin is in the center of the chip, unit: μm

Pad No	Name	X	Y	Pad No	Name	X	Y
1	COM0	93.11	1016.655	17	SEG12	1056.89	1621.89
2	COM1	93.11	932.155	18	SEG13	1056.89	1265.89
3	COM2	93.11	847.655	19	SEG14	1056.89	1350.39
4	COM3	93.11	763.155	20	SEG15	1040.39	1621.89
5	COM4/SEG0	130.97	93.11	21	SEG16	950.39	1621.89
6	COM5/SEG1	220.97	93.11	22	SEG17	860.39	1621.89
7	COM6/SEG2	310.9	93.11	23	SEG18	756.75	1621.89
8	COM7/SEG3	400.97	93.11	24	SEG19	666.75	1621.89
9	SEG4	490.97	93.11	25	VLCD	576.75	1621.89
10	SEG5	580.97	93.11	26	VCCA2	486.75	1621.89
11	SEG6	670.97	93.11	27	VDD	396.75	1621.89
12	SEG7	760.97	93.11	28	SDA	306.75	1621.89
13	SEG8	850.97	93.11	29	SCL	199.61	1621.89
14	SEG9	940.97	93.11	30	VSS	109.61	1621.89
15	SEG10	1030.97	93.11				
16	SEG11	1056.89	1096.89	0	TEST	295.57	1211.795

6 Pinouts and pin description



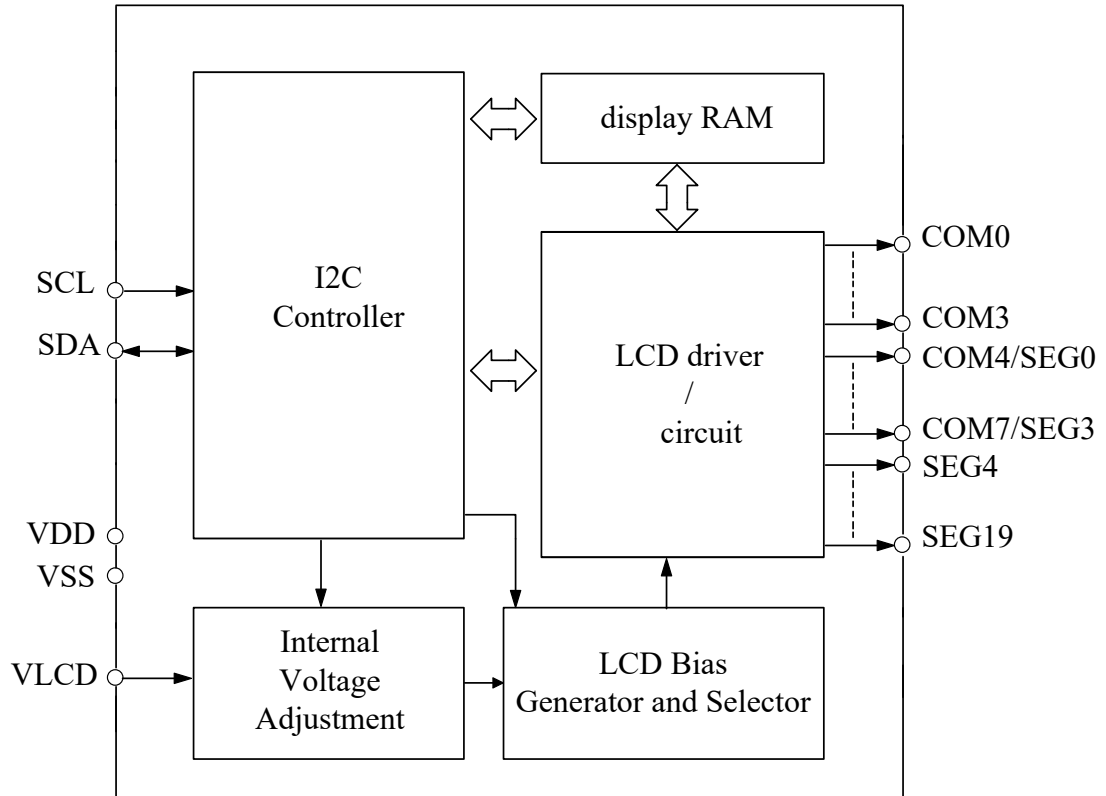
For more information: [Page 21](#)

6.1 VK2C21A/SOP28 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM outputs , software configuration 4COM or 8COM
13-27	SEG4-SEG18	O	LCD SEG outputs
28	SEG19/VLCD	I/O	<p>VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation.</p> <p>VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.</p>

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The static display memory (RAM) structure is 16×8 bits (20×4 bits for 4COM), which stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Access the data in the display RAM through the I2C command.

The following is a mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					0x00
SEG3					SEG2					0x01
SEG5					SEG4					0x02
SEG7					SEG6					0x03
SEG9					SEG8					0x04
SEG11					SEG10					0x05
SEG13					SEG12					0x06
SEG15					SEG14					0x07
SEG17					SEG16					0x08
SEG19					SEG18					0x09
Data	Bit7	Bit6	Bit5	Bit4		Bit3	Bit2	Bit1	Bit0	

RAM Mapping of 20×4

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	Address
SEG4									0x00
SEG5									0x01
SEG6									0x02
SEG7									0x03
SEG8									0x04
SEG9									0x05
SEG10									0x06
SEG11									0x07
SEG12									0x08
SEG13									0x09
SEG14									0x0A
SEG15									0x0B
SEG16									0x0C
SEG17									0x0D
SEG18									0x0E
SEG19									0x0F
Data	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

RAM Mapping of 16×8

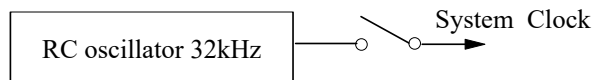
7.3 System Oscillator

The clock of VK2C21A is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (fSYS) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driving voltage can be obtained through the VLCD pins or by selecting 16 levels of voltage through the internal configuration.

The VDD pad is connected to the VCCA2 pad, and the driving voltage of the LCD is obtained by connecting a resistor in series with the VLCD to the VDD ($VLCD \leq VDD$).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table:

DA3~DA0 \ Bias	1/3	1/4	Note
0x00	1.000×VDD	1.000×VDD	Default
0x01	0.944×VDD	0.957×VDD	
0x02	0.894×VDD	0.918×VDD	
0x03	0.849×VDD	0.882×VDD	
0x04	0.808×VDD	0.849×VDD	
0x05	0.771×VDD	0.818×VDD	
0x06	0.738×VDD	0.789×VDD	
0x07	0.707×VDD	0.763×VDD	
0x08	0.678×VDD	0.738×VDD	
0x09	0.652×VDD	0.714×VDD	
0x0A	0.628×VDD	0.692×VDD	
0x0B	0.605×VDD	0.672×VDD	
0x0C	0.584×VDD	0.652×VDD	
0x0D	0.565×VDD	0.634×VDD	
0x0E	0.547×VDD	0.616×VDD	
0x0F	0.529×VDD	0.600×VDD	

7.5 Power-On Reset

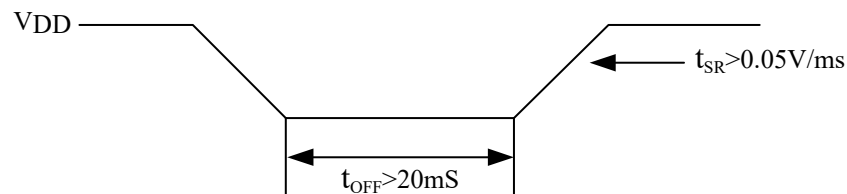
The power-on reset circuit is initialized. During this period (1ms), I2C should not transmit data.

The state of the internal circuit after initialization is as follows:

- All COM/SEG pins are output as VLCD.
- Display modes 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- LCD display off.
- The internal voltage adjustment function is enabled.
- The SEG/VLCD shared pin is set as the SEG pin.
- The VLCD foot detection function is disabled.
- The frame rate is set to 80Hz by default.
- The flashing function is disabled.

During the operation of the chip, if the VDD drops below the specified minimum operating voltage, the power-on reset timing condition must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing:



7.6 LCD Communication Command

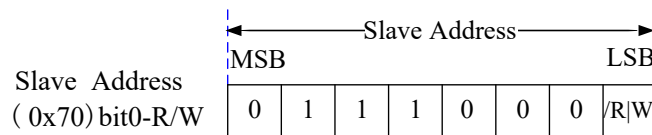
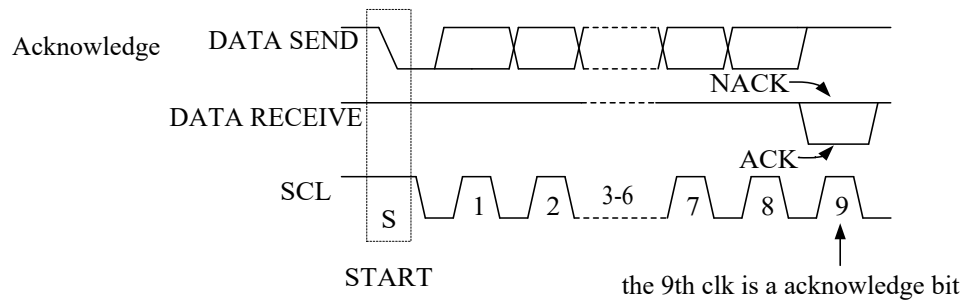
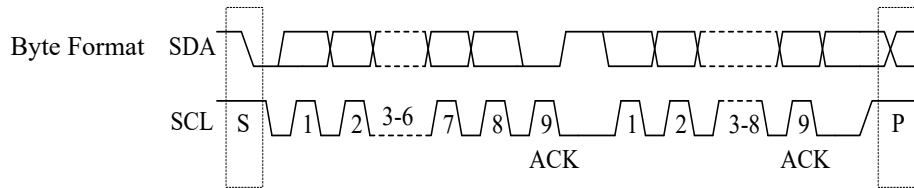
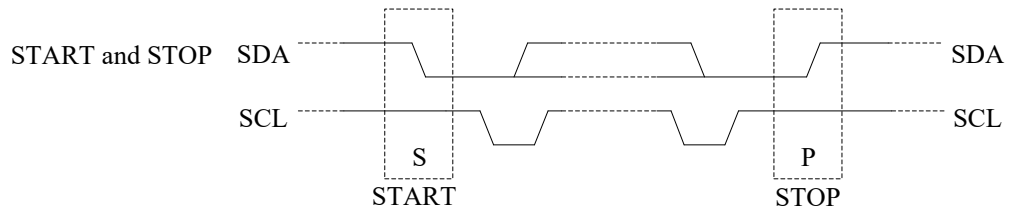
The display modes supported by the LCD driver are 20SEG×4COM and 16SEG×8COM. The unused SEG and COM pins are left floating.

Two frame rates are provided. You can choose between 80Hz and 160Hz through the frame rate setting command.

8 I2C Serial Interface

The VK2C21A has two communication pins and follows the I2C protocol. For open-drain output, an external pull-up resistor needs to be connected.

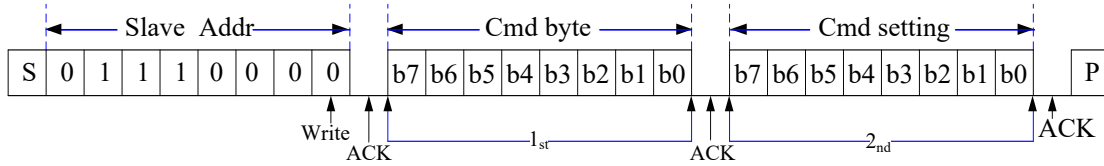
The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both of these pins are at a high level.



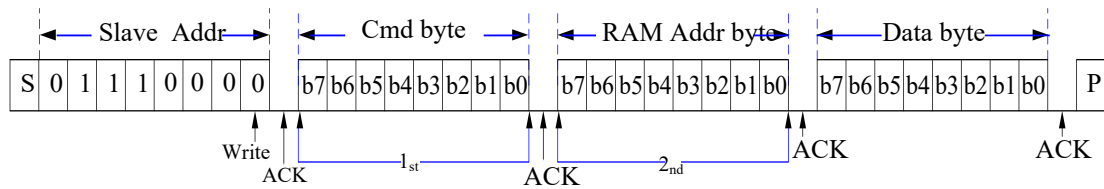
9 I2C Command Format

Write Operation

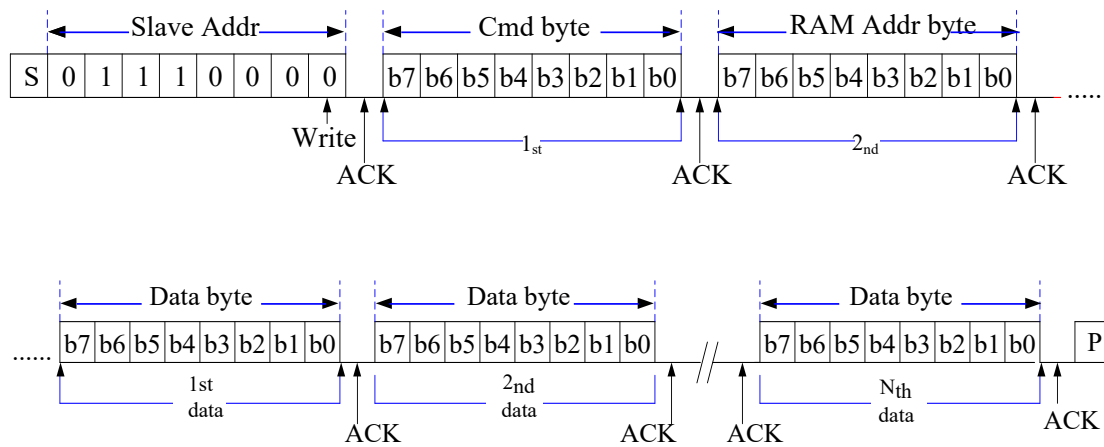
Byte Writes Operation



Display RAM Single Data Byte

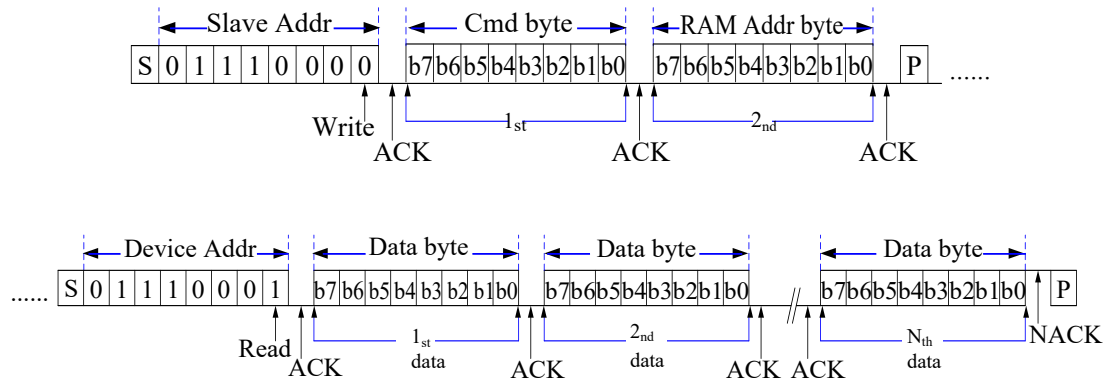


Display RAM Page Write Operation

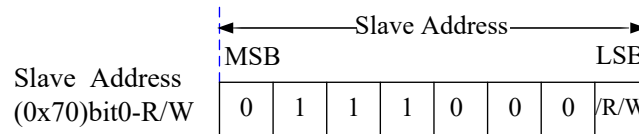


Read Operation

Display RAM Page Read Operation



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
mode set cmd	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

10.3 System Set Command

Set the internal system oscillator on/off and display on/off.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
system set cmd	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/off set	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	internal oscillator	LCD on/off
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

10.4 Frame Frequency Command

Selects the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
frame freq cmd	1st	1	0	0	0	0	1	1	0		W	
frame freq set	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame Frequency
F	
0	80Hz
1	160Hz

10.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq cmd	1st	1	0	0	0	1	0	0	0		W	
blinking freq set	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

10.6 Internal Voltage Set Command

The internal voltage adjustment can provide sixteen kinds of regulator voltage adjustment options.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA cmd	1 st	1	0	0	0	1	0	1	0		W	
IVA set	2 nd	X	X	DE	VE	DA3	DA2	DA1	DA0	SEG/VLCD 引脚功能通过 DE位设置。 VE位使能或禁止内部电压调整功能。 DA3~DA0 用来调整VLCD 输出电压。	W	30H

Note:

Bit 5	Bit 4	SEG19/VLCD shared pin sel	internal voltage adjustment	Note
DE	VE			
0	0	VLCD pin	off	<ul style="list-style-type: none"> • SEG/VLCD pin is set as the VLCD pin • Disable internal voltage adjustment function • An external resistor is connected in series between the VLCD pin and the VDD pin to adjust the bias voltage. At the same time, the DA3-DA0 bit must be set to a value other than "0000" to enable the internal voltage follower. • VLCD pin is connected to the VDD pin, the internal voltage must be disabled by set DA3~DA0 as "0000".
0	1	VLCD pin	on	<ul style="list-style-type: none"> • SEG/VLCD pin is set as the VLCD pin • Enable internal voltage adjustment function • The VLCD pin is an output pin, and the voltage of the VLCD pin is detected by the MCU.
1	0	SEG19 pin	off	<ul style="list-style-type: none"> • SEG/VLCD pin is set as the segment pin • Disable internal voltage adjustment function. • The bias voltage is provided by internal VDD. • Regardless of the value of DA3-DA0, the internal voltage follower is prohibited.
1	1	SEG19 pin	on	<ul style="list-style-type: none"> • SEG/VLCD pin is set as the segment pin • Enable internal voltage adjustment function

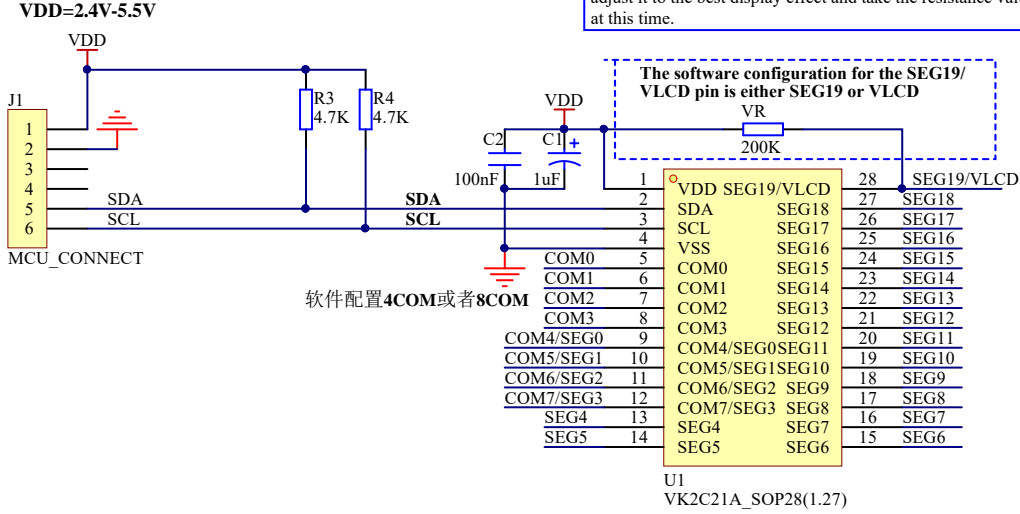
- Power-on: Enable internal voltage Adjustment and the SEG/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to "0000", the internal voltage is disabled.
- When the DA0~DA3 bits are set to other values except "0000", internal voltage follower is enabled.

11 Application Circuits

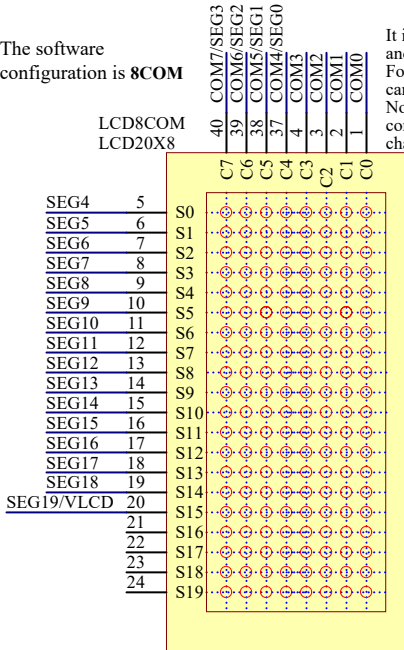
When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin

When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin

The software configuration of SEG19/VLCD pins is VLCD
When VDD=5V and VR=200K:
The VLCD is approximately 4.2V
It is recommended to use a 510K adjustable resistor for VR to adjust it to the best display effect and take the resistance value at this time.



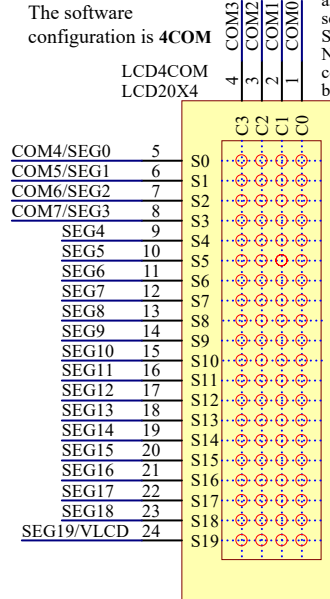
The software configuration is 8COM



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence. For the convenience of PCB routing, the SEG pins can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

RAM0-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM1-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM2-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM3-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM4-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM5-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM6-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM7-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM8-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM9-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM10-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM11-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM12-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM13-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM14-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RAM15-BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

The software configuration is 4COM



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence. For the convenience of PCB routing, the SEG pins can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

RAM0-BIT3	BIT2	BIT1	BIT0
RAM1-BIT3	BIT2	BIT1	BIT0
RAM2-BIT3	BIT2	BIT1	BIT0
RAM3-BIT3	BIT2	BIT1	BIT0
RAM4-BIT3	BIT2	BIT1	BIT0
RAM5-BIT3	BIT2	BIT1	BIT0
RAM6-BIT3	BIT2	BIT1	BIT0
RAM7-BIT3	BIT2	BIT1	BIT0
RAM8-BIT3	BIT2	BIT1	BIT0
RAM9-BIT3	BIT2	BIT1	BIT0
RAM10-BIT3	BIT2	BIT1	BIT0
RAM11-BIT3	BIT2	BIT1	BIT0
RAM12-BIT3	BIT2	BIT1	BIT0
RAM13-BIT3	BIT2	BIT1	BIT0
RAM14-BIT3	BIT2	BIT1	BIT0
RAM15-BIT3	BIT2	BIT1	BIT0

12 Electrical characteristics

12.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3~6.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Storage Temperature	T _{STG}	-50~+125	°C
Operating Temperature	T _{OTG}	-40~+85	°C

12.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	IDD1	—	18	27	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	25	40		5V	
Operating current	IDD2	—	2	5	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	ISTB	—	0.1	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	0.3	2		5V	
Input Low Voltage	VIL	0	—	0.3	VDD	3V	SCL, SDA
						5V	
Input High Voltage	VIH	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	IOL	3.0	—	—	mA	3V	VOL=0.4V, SDA
		6.0	—	—		5V	
LCD COM Sink Current	IOL1	250	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD COM Source Current	IOH1	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V
LCD SEG Sink Current	IOL2	2500	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD SEG Source Current	IOH2	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V

12.3 AC Characteristics

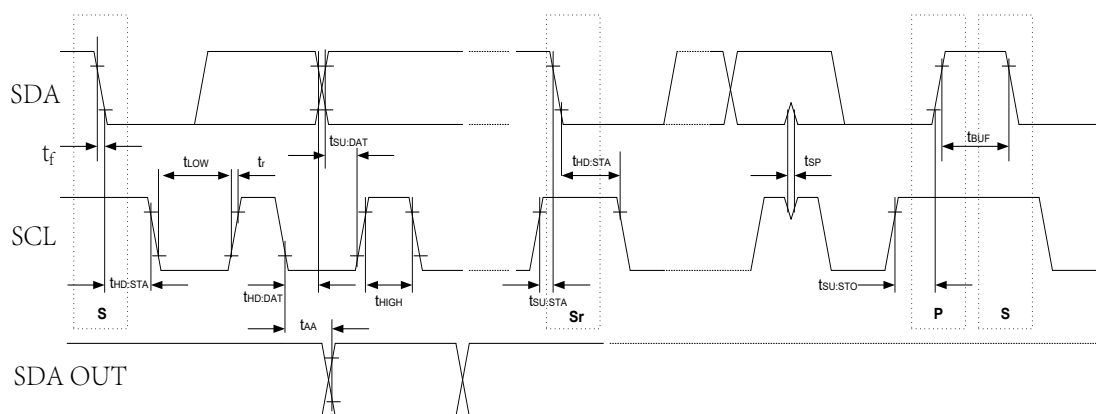
Frame Frequency

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	f _{LCD1}	72	80	88	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD2}	144	160	176	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD3}	52	80	124	Hz	4.0V	1/4 duty, -40 ~ +85°C
LCD Frame Frequency	f _{LCD4}	104	160	248	Hz	4.0V	1/4 duty, -40 ~ +85°C

I2C parameter

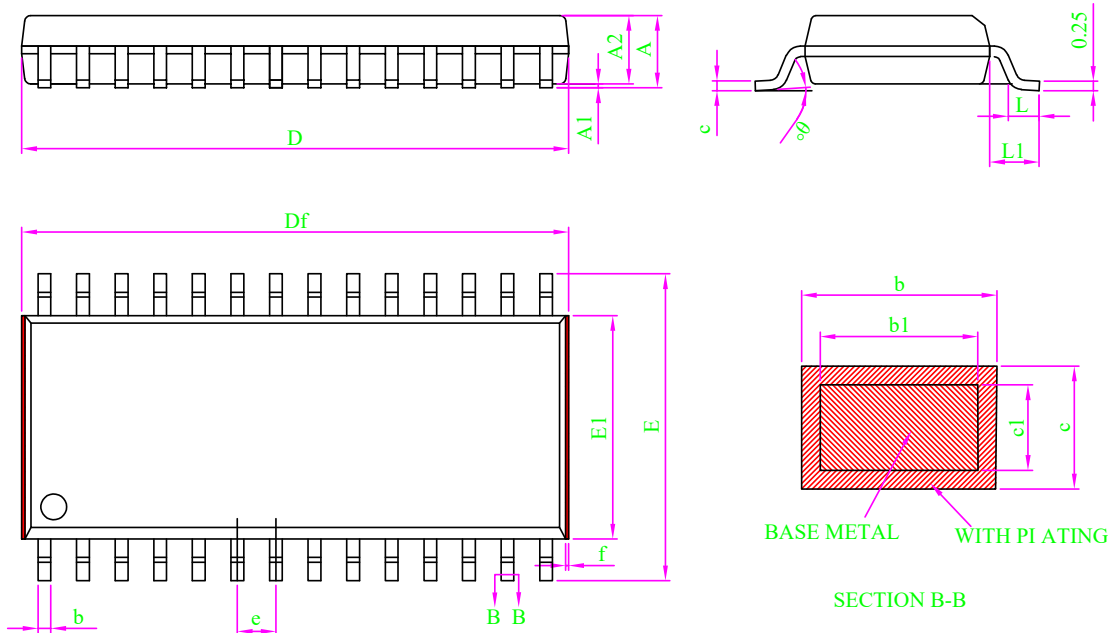
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f _{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t _{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	t _{HD:STA}	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t _{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t _{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	t _{SU:STA}	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	t _{HD:DAT}	0	—	—	ns	3.0-5.5V	—
Data Setup Time	t _{SU:DAT}	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t _R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t _F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	t _{SU:STO}	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	t _{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t _{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C 时序



14 封装信息

14.1 SOP28 (300mil)(18mm×7.5mm PP=1.27mm)



Note:

1. All dimension are in m
2. Dim D& E1 does not include plast flas; Df includes plastic flash(f);Flash: Plastic residual around body edge after de junk / singulation.
3. Dim b does not include damb protrusion/intrusion.
4. Plating thickness 0.007mm-0.020mm

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.64
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	-	0.47
b1	0.38	0.41	0.43
c	0.25	-	0.30
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
Df	18.00	-	18.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.71	0.86	1.01
L1	1.30	1.40	1.50
θ	0	-	8°
f	0.05	-	0.20

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Check alignment	YES
4	1.3	2025-05-18	Update version	YES

[1] Consult the recently published documents before starting or finishing the design.

[2] Since the release of this document , the device product status described in this document may have changed and may differ in several cases. The latest product status information can be found on the Internet at <https://www.szvinka.com/>