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VK2C23B Datasheet

35×8 LCD DRIVER

Rev.1.3

1 General Description

The VK2C23B is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 280 dots (35SEG×8COM) . The single-chip microcomputer can be configured with display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as various industrial control instruments.

2 Key Features

- Operating voltage：2.4-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias: 1/3 or 1/4
- Selectable LCD duty: 1/8
- Built-in 56×4-bit、52×8-bit bit display RAM
- The frame rate can be configured as 80Hz or 160Hz
- Power-down mode via software command(LCD OFF, SYS DIS)
- I2C communication interface
- Display mode 35×8
- Three display overall flicker frequencies
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides the LCD driving voltage source(2.4-5.5V)
- It is equipped with a built-in 16-stage LCD driver voltage adjustment circuit
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
  LQFP48(7.0mm × 7.0mm PP=0.5mm)
  DICE
  COG

3 Product Selection

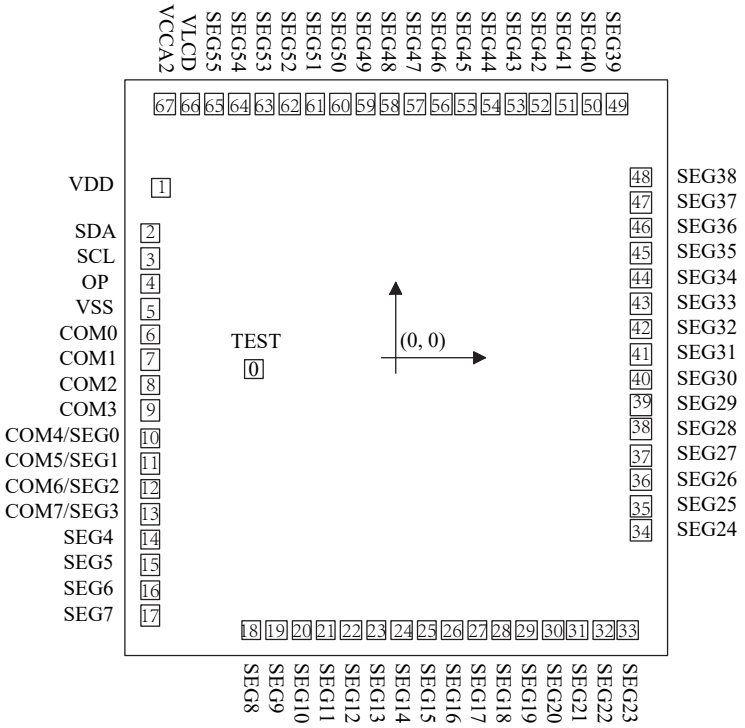
Part No.	SEG×COM	BIAS	DUTY	Packaging
VK2C21A	20×4,16×8	1/3,1/4	1/4,1/8	SOP28
VK2C21AA	20×4,16×8	1/3,1/4	1/4,1/8	SSOP28
VK2C21AQ	20×4,16×8	1/3,1/4	1/4,1/8	QFN28L
VK2C21B	16×4,12×8	1/3,1/4	1/4,1/8	SOP24
VK2C21BA	16×4,12×8	1/3,1/4	1/4,1/8	SSOP24
VK2C21BQ	16×4,12×8	1/3,1/4	1/4,1/8	QFN24L
VK2C21C	12×4,8×8	1/3,1/4	1/4,1/8	SOP20
VK2C21CQ	12×4,8×8	1/3,1/4	1/4,1/8	QFN20L
VK2C21D	8×4,4×8	1/3,1/4	1/4,1/8	SOP16
VK2C21DQ	8×4,4×8	1/3,1/4	1/4,1/8	QFN16L
VK2C22A	44×4	1/2,1/3	1/4	LQFP52
VK2C22B	40×4	1/2,1/3	1/4	LQFP48
VK2C22	44×4	1/2,1/3	1/4	DICE
VK2C23A	55×4,51×8	1/3,1/4	1/4, 1/8	LQFP64
VK2C23B	35×8	1/3,1/4	1/8	LQFP48
VK2C23	56×4,52×8	1/3,1/4	1/4,1/8	DICE
VK2C24A	71×4,67×8,59×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP80
VK2C24B	55×4,51×8,43×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP64
VK2C24	72×4,68×8,60×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	DICE

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK2C21A	SOP28	26/tube	-	2080/box	20800 PCS	
VK2C21AA	SSOP28	50/tube	-	5000/box	50000 PCS	
VK2C21AQ	QFN28L	-	490/reel	4900/box	29400 PCS	
VK2C21B	SOP24	30/tube	-	2400/box	24000 PCS	
VK2C21BA	SSOP24	50/tube	-	10000/box	100000 PCS	
VK2C21BQ	QFN24L	-	490/reel	4900/box	29400 PCS	
VK2C21C	SOP20	36/tube	-	2880/box	28800 PCS	
VK2C21CQ	QFN20L	-	490/reel	4900/box	29400 PCS	
VK2C21D	SOP16	50/tube	-	10000/box	100000 PCS	
VK2C21DQ	QFN16L	-	3000/reel	3000/box	120000 PCS	
VK2C22A	LQFP52	-	90/tray	900/box	5400 PCS	
VK2C22B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C22	DICE	-	400/tray	2000/box	4000 PCS	DICE
VK2C23A	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C23B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C23	DICE	-	250/tray	1000/box	2000 PCS	DICE
VK2C24A	LQFP80	-	90/tray	900/box	5400 PCS	
VK2C24B	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C24	DICE	-	200/tray	1000/box	2000 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip size: 1750×1920 μ m ², substrate potential: VSS
PAD size: 70×70 um, spacing: 113 um, aluminum pad size: 100×100 um,
aluminum pad thickness: 1.2um
When VLCD pad and VCCA2 pad are bound together, VLCD ≤+5.5V(VLCD can be connected to an external voltage source to achieve VLCD≥VDD)

Built-in voltage setting (IVA) command		VLCD	SEG55	Notes
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Input	Null	• The internal voltage is adjusted to Null • VLCD supports internal bias voltage
1	0	Input	Output	• VLCD supports internal bias voltage
1	1	Input	Output	• VLCD supports internal bias voltage

When VDD pad and VCCA2 pad are bound together, VLCD ≤ VDD

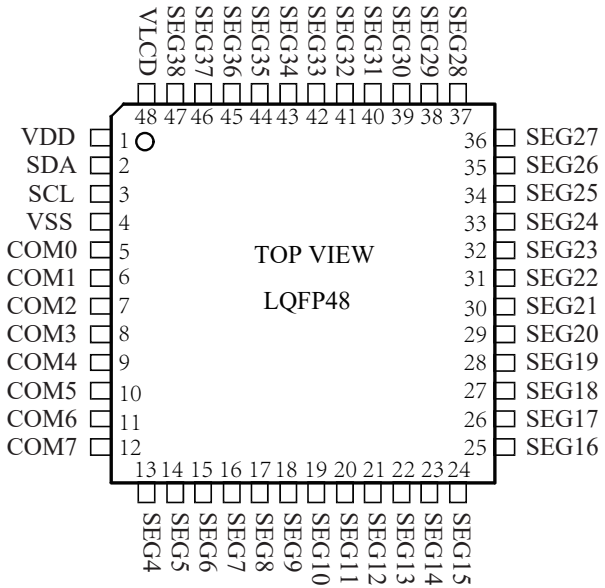
Built-in voltage setting (IVA) command		VLCD	SEG55	Notes
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Output	Null	• Detect the internal bias voltage *1 • VDD supports internal bias voltage
1	0	NC	Output	• VDD supports internal bias voltage
1	1	NC	Output	• VDD supports internal bias voltage

5.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	VDD	103.11	1887.01	35	SEG25	2021.89	488.19
2	SDA	98.11	1736.67	36	SEG26	2021.89	593.19
3	SCL	98.11	1623.17	37	SEG27	2021.89	698.19
4	OP	98.11	1518.17	38	SEG28	2021.89	803.19
5	VSS	103.11	1413.17	39	SEG29	2021.89	908.19
6	COM0	98.11	1308.17	40	SEG30	2021.89	1013.19
7	COM1	98.11	1203.17	41	SEG31	2021.89	1118.19
8	COM2	98.11	1098.17	42	SEG32	2021.89	1223.19
9	COM3	98.11	993.17	43	SEG33	2021.89	1328.19
10	COM4/SEG0	98.11	888.17	44	SEG34	2021.89	1433.19
11	COM5/SEG1	98.11	783.17	45	SEG35	2021.89	1538.19
12	COM6/SEG2	98.11	1724.57	46	SEG36	2021.89	1643.19
13	COM7/SEG3	98.11	573.17	47	SEG37	2021.89	1748.19
14	SEG4	98.11	468.17	48	SEG38	2021.89	1853.19
15	SEG5	98.11	363.17	49	SEG39	1973.75	2191.89
16	SEG6	98.11	258.17	50	SEG40	1868.75	1868.75
17	SEG7	98.11	153.17	51	SEG41	1763.75	2191.89
18	SEG8	359.57	98.11	52	SEG42	1658.75	2191.89
19	SEG9	464.57	98.11	53	SEG43	1553.75	2191.89
20	SEG10	569.57	98.11	54	SEG44	1448.75	2191.89
21	SEG11	674.57	98.11	55	SEG45	1343.75	2191.89
22	SEG12	779.57	98.11	56	SEG46	1238.75	2191.89
23	SEG13	884.57	98.11	57	SEG47	1133.75	2191.89
24	SEG14	989.57	98.11	58	SEG48	1028.75	2191.89
25	SEG15	1094.57	98.11	59	SEG49	923.75	2191.89
26	SEG16	1199.57	98.11	60	SEG50	818.75	2191.89
27	SEG17	1304.57	98.11	61	SEG51	713.75	2191.89
28	SEG18	1409.57	98.11	62	SEG52	608.75	2191.89
29	SEG19	1514.57	98.11	63	SEG53	503.75	2191.89
30	SEG20	1619.57	98.11	64	SEG54	392.75	2191.89
31	SEG21	1724.57	98.11	65	SEG55	287.75	2191.89
32	SEG22	1829.57	98.11	66	VLCD	182.75	1452.16
33	SEG23	1934.57	98.11	67	VCCA2	77.75	2191.89
34	SEG24	2021.89	383.19	0	TEST	629.32	1452.16

6 Package Pinout Information(LQFP48)



Note: LCD 1/4 duty is not supported

The VCCA2 pad is internally connected to the VLCD pad, the OP pad is left floating(NC)

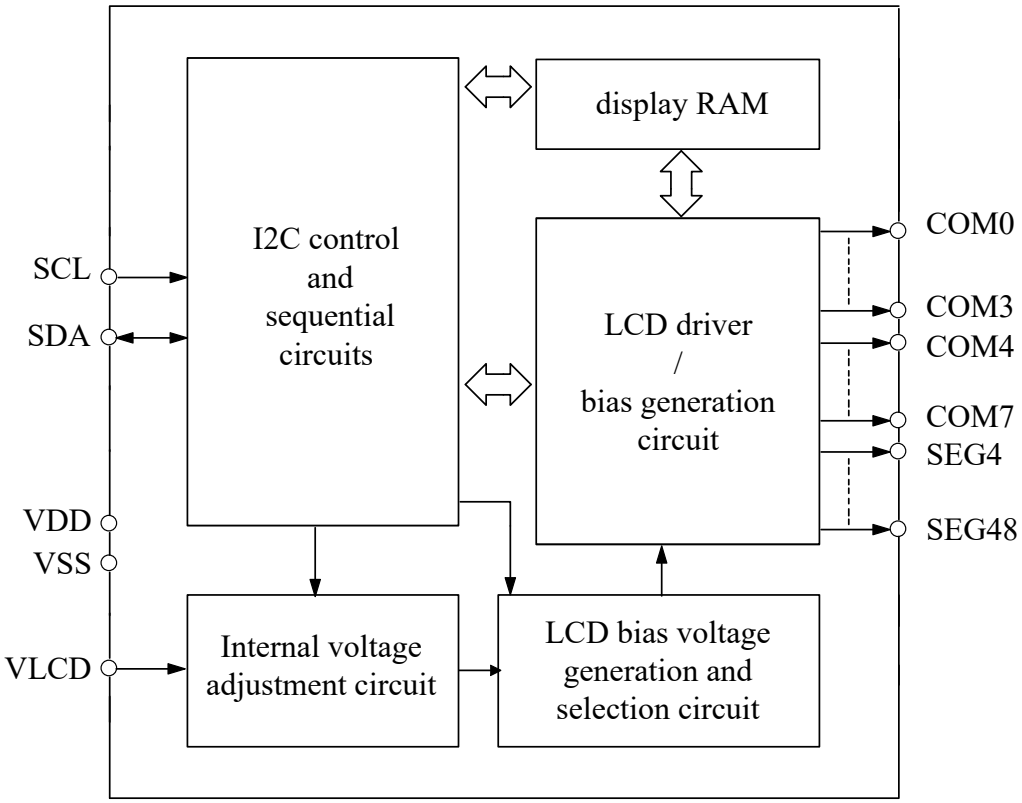
For more information: Page 23

6.1 VK2C23B/LQFP48 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-12	COM0-COM7	O	LCD COM drive outputs
13-47	SEG4-SEG38	O	LCD SEG drive outputs
48	VLCD	I	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The display RAM is organized as 52×8 bits and stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Display RAM data is accessed via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	Address
SEG4									0x00
SEG5									0x01
SEG6									0x02
SEG7									0x03
SEG8									0x04
SEG9									0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG38									0x22
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
---									0x33
Data	bit7	bit6	bit5	bit4	bit3	bit22	bit1	bit0	

RAM Mapping of 52×8

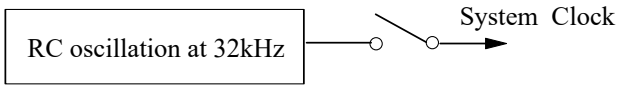
7.3 System Oscillator

The clock of VK2C23B is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (f_{SYS}) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driver voltage can be obtained through the VLCD pin or selected as a 16-level voltage through the internal configuration.

When the VLCD pad is connected to the VCCA2 pad, the LCD driving voltage can be supplied from an external voltage source (VLCD≤5.5V),and VLCD may be higher than VDD.

When the VDD pad is connected to the VCCA2 pad, the LCD driving voltage can be obtained by connecting the VLCD pin to VDD through a series resistor (VLCD≤VDD).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table: when the VCCA2 pad is connected to the VDD pad

Bias / DA3~DA0	1/3	1/4	Note
0x00	1.000×VDD	1.000×VDD	Default
0x01	0.944×VDD	0.957×VDD	
0x02	0.894×VDD	0.918×VDD	
0x03	0.849×VDD	0.882×VDD	
0x04	0.808×VDD	0.849×VDD	
0x05	0.771×VDD	0.818×VDD	
0x06	0.738×VDD	0.789×VDD	
0x07	0.707×VDD	0.763×VDD	
0x08	0.678×VDD	0.738×VDD	
0x09	0.652×VDD	0.714×VDD	
0x0A	0.628×VDD	0.692×VDD	
0x0B	0.605×VDD	0.672×VDD	
0x0C	0.584×VDD	0.652×VDD	
0x0D	0.565×VDD	0.634×VDD	
0x0E	0.547×VDD	0.616×VDD	
0x0F	0.529×VDD	0.600×VDD	

When the VCCA2 pad is connected to the VLCD pad

Bias / DA3~DA0	1/3	1/4	Note
0x00	1.000×VLCD	1.000×VLCD	Default
0x01	0.944×VLCD	0.957×VLCD	
0x02	0.894×VLCD	0.918×VLCD	
0x03	0.849×VLCD	0.882×VLCD	
0x04	0.808×VLCD	0.849×VLCD	
0x05	0.771×VLCD	0.818×VLCD	
0x06	0.738×VLCD	0.789×VLCD	
0x07	0.707×VLCD	0.763×VLCD	
0x08	0.678×VLCD	0.738×VLCD	
0x09	0.652×VLCD	0.714×VLCD	
0x0A	0.628×VLCD	0.692×VLCD	
0x0B	0.605×VLCD	0.672×VLCD	
0x0C	0.584×VLCD	0.652×VLCD	
0x0D	0.565×VLCD	0.634×VLCD	
0x0E	0.547×VLCD	0.616×VLCD	
0x0F	0.529×VLCD	0.600×VLCD	

7.5 Power-On Reset

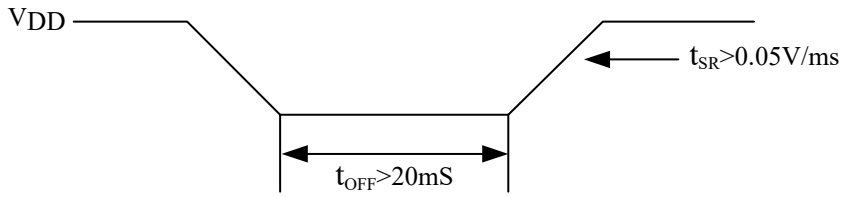
During the initialization of the power-on reset circuit(1ms),no I2C data transmission should occur.

The state of the internal circuit after initialization is as follows:

- When VLCD≤VDD, all COM/SEG pins output VDD
- When VDD≤VLCD, all COM/SEG pins output VLCD
- The default configuration of the LQFP64 package is 1/4 duty and 1/3 bias.
- The LQFP48 package is default configured with 1/8 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- LCD display off.
- The internal voltage adjustment function is enabled.
- Set the shared pin of SEG/VLCD as the SEG pin.
- The VLCD pin detection function is prohibited.
- The default frame rate is configured to 80Hz.
- The flashing function is disabled.

If,during operation, VDD falls below the specified minimum operating voltage, the power-on reset timing requirements must be met,that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing:



7.6 LCD Communication Command

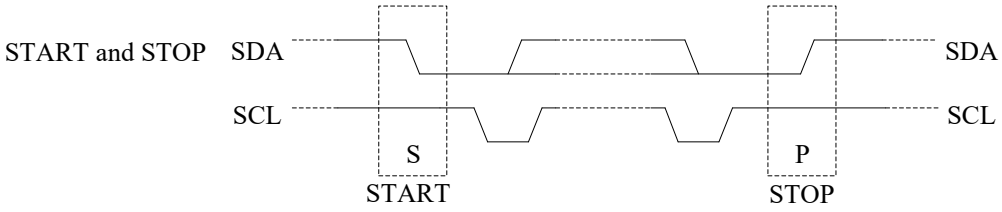
The LCD driver supports 35SEG×8COM modes, any unused SEG and COM pins should be left floating(NC).

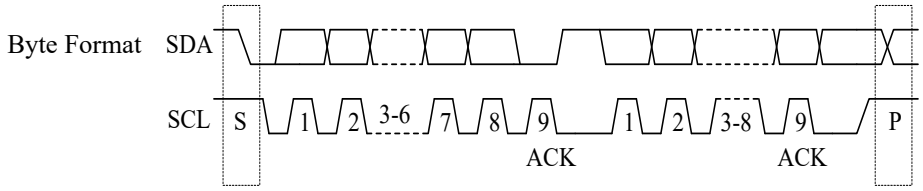
Two frame frequencies are provided, and you can choose to set them to 80Hz or 160Hz through the frame frequency setting command.

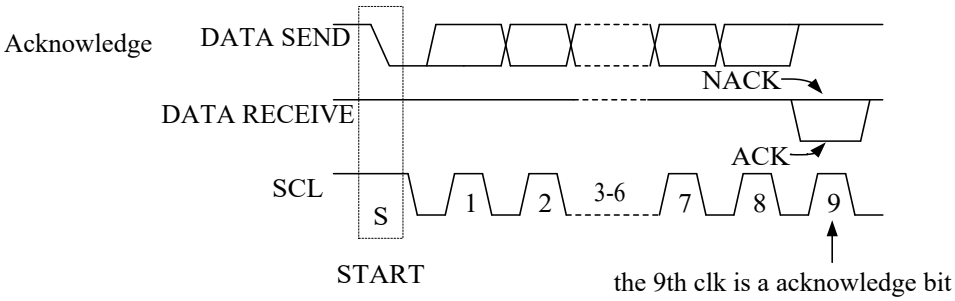
8 I2C Serial Interface

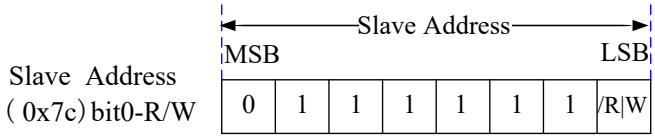
The VK2C23B features two communication pins compliant with the I2C protocol. open-drain outputs require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both pins remain at a logic high level.





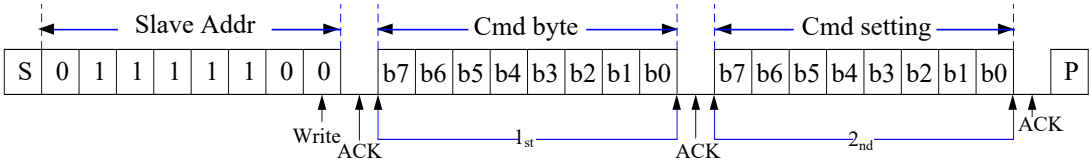




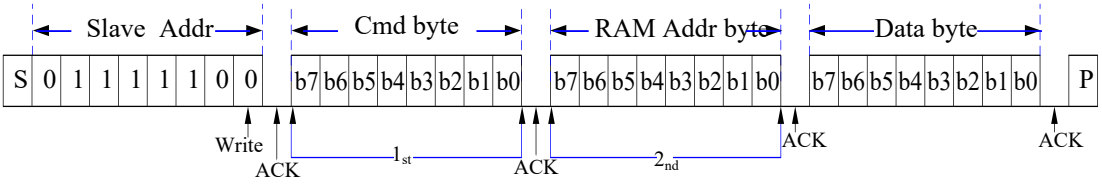
9 I2C Command Format

Write operation

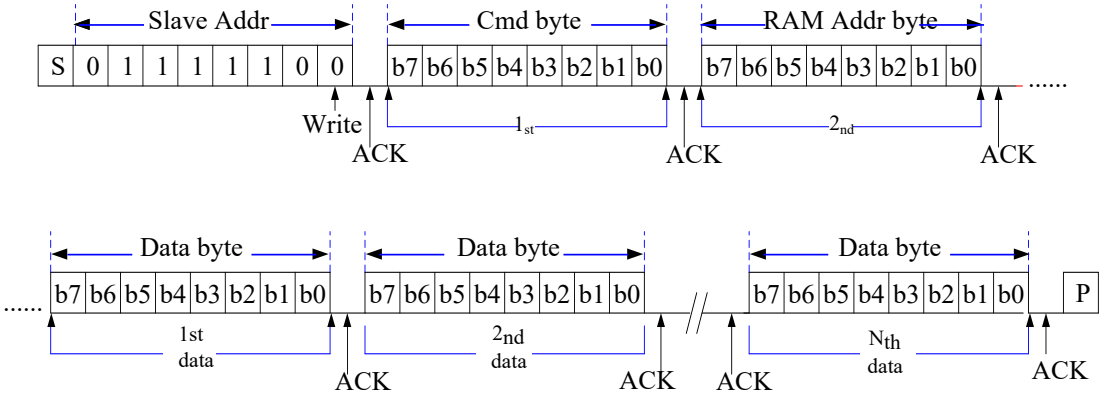
Write commands



Write a single byte to the display RAM

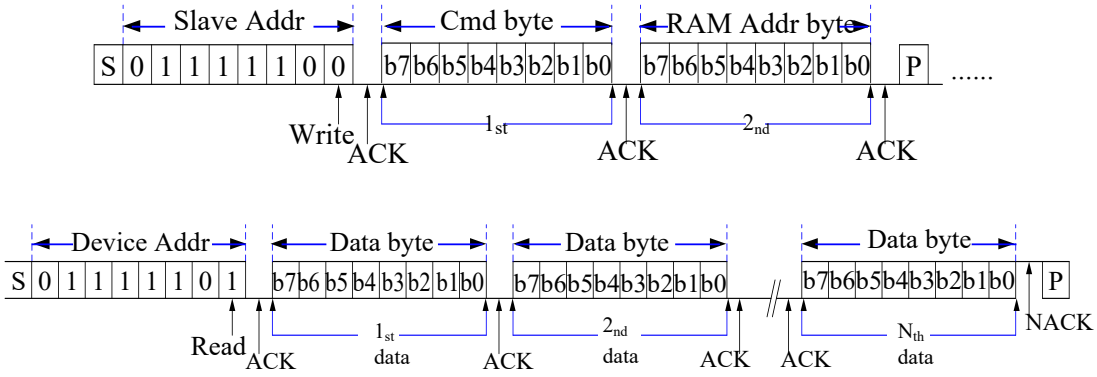


Write multiple bytes to the display RAM

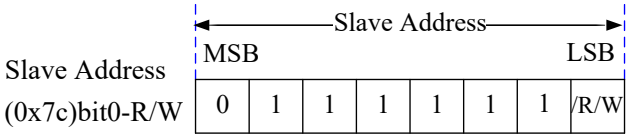


Read operation

Read multiple bytes from the display RAM



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Mode setting command	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

10.3 System Settings Command

Enable/disable the internal system oscillator and LCD display

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
System Settings Command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and display on/off Settings	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	Internal system oscillator	LCD display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

10.4 Frame rate setting command

Select the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame frequency
F	
0	80Hz
1	160Hz

10.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Blinking frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	4Hz
1	0	2Hz
1	1	1Hz

10.6 Internal Voltage Adjustment(IVA) Command

The IVA command allows selection of 16 voltage levels to adjust the LCD driver voltage

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA Com	1st	1	0	0	0	1	0	1	0		W	
IVA set	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	The SEG/VLCD pin function is set through the DE bit. The VE bit enables or disables the internal voltage adjustment function. DA3 to DA0 are used to adjust the output voltage of the VLCD.	W	30H

Note：

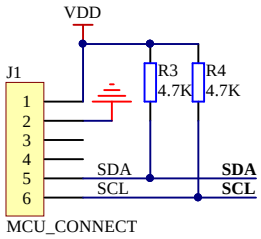
Bit 5	Bit 4	SEG55/VLCD shared pin sel	internal voltage adjustment	Note
DE	VE			
0	0	VLCD pin	off	• VCCA2→VLCD: bias voltage is provided by VLCD pin • VCCA2→VDD: bias voltage is provided by VLCD pin. • Note:VLCD→VDD: disable the internal voltage follower by setting DA3- DA0 to "0000".
0	1	VLCD pin	on	• VCCA2→VLCD: Internal voltage adjustment disabled. (bias voltage is provided by VLCD pin) • VCCA2→VDD:bias voltage is provided by VLCD • pin,Internal adjustment disabled. (Not recommended.) • VCCA2→VDD:VLCD floating,Internal adjustment enabled. (internal regulation adjusts bias)
1	0	SEG55 pin/COB	off	• VCCA2→VLCD: bias voltage is provided by VLCD pin • VCCA2→VDD: bias voltage is provided by VDD pin. Note:Internal voltage follower is automatically disabled, ignore DA3 to DA0 bits.
1	1	SEG55 pin/COB	on	• VCCA2→VLCD: bias voltage is provided by VLCD,internal regulation adjusts bias. • VCCA2→VDD:bias voltage is provided by VDD,internal regulation adjusts bias.

- Power-on status: The internal voltage adjustment function is enabled and the SEG/VLCD pin is selected as the SEG pin.
- When the DA0 to DA3 bits are set to "0000", the internal voltage follower is prohibited.
- When the DA0 to DA3 bits are set to values other than "0000", the internal voltage follower is enabled.

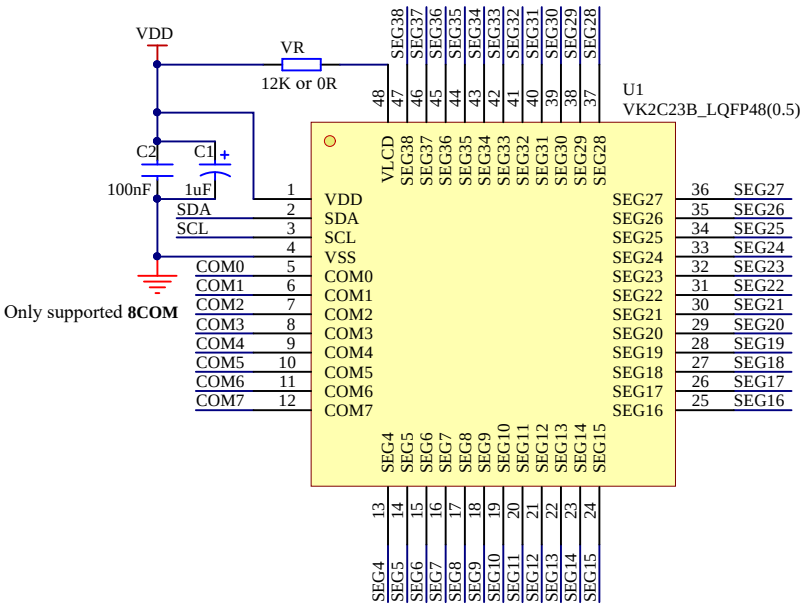
11 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin

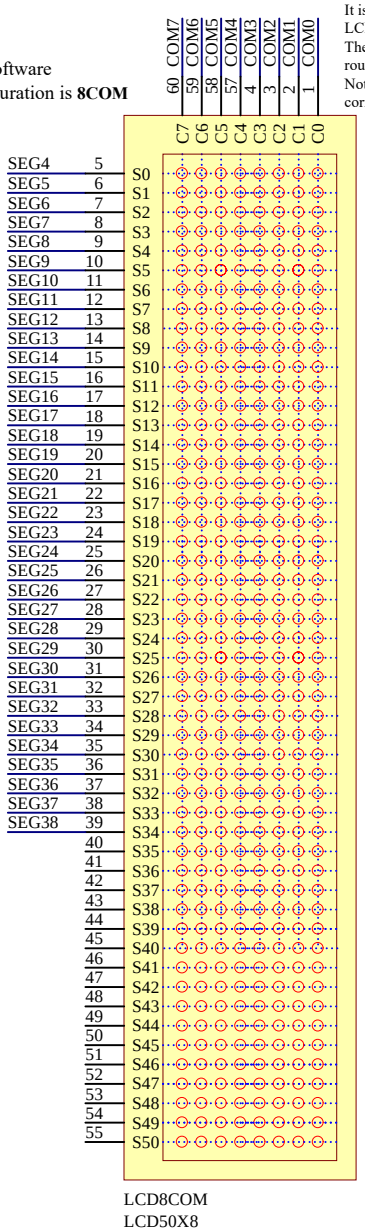
VDD=2.4V-5.5V



1. The software configuration bias voltage is achieved through the internal voltage adjustment function: VLCD and VDD are short-circuited, with VR=0R
2. When the software configuration bias voltage is provided by the VLCD pin:
(VLCD can be connected to a power supply less than 5.5V through VR, and VLCD can be larger than VDD.
When VLCD is connected to VDD via VR, with VDD=5V and VR=12K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.



The software configuration is **8COM**



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

RAM0-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM1-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM2-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM3-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM4-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM5-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM6-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM7-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM8-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM9-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM10-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM11-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM12-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM13-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM14-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM15-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0

RAM33-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM34-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I_{DD1}	—	18	40	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	25	50		5V	
Operating current	I_{DD2}	—	2	5	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I_{STB}	—	0.1	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	0.3	2		5V	
Low-level Input	V_{IL}	0	—	0.3	VDD	3V	SCL, SDA
						5V	
High-level Input	V_{IH}	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I_{OL}	3.0	—	—	mA	3V	V_{OL}=0.4V，SDA
		6.0	—	—		5V	
LCD COM Sink Current	I_{OL1}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V

13 AC Electrical Characteristics

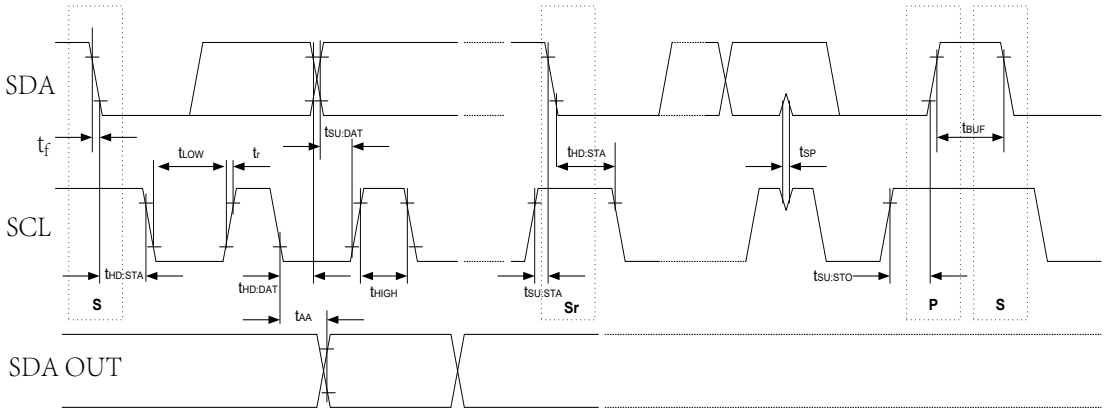
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	fLCD1	72	80	88	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD2	144	160	176	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD3	52	80	124	Hz	4.0V	1/4 duty,-40 ~ +85℃
LCD Frame Frequency	fLCD4	104	160	248	Hz	4.0V	1/4 duty,-40 ~ +85℃

I2C parameter

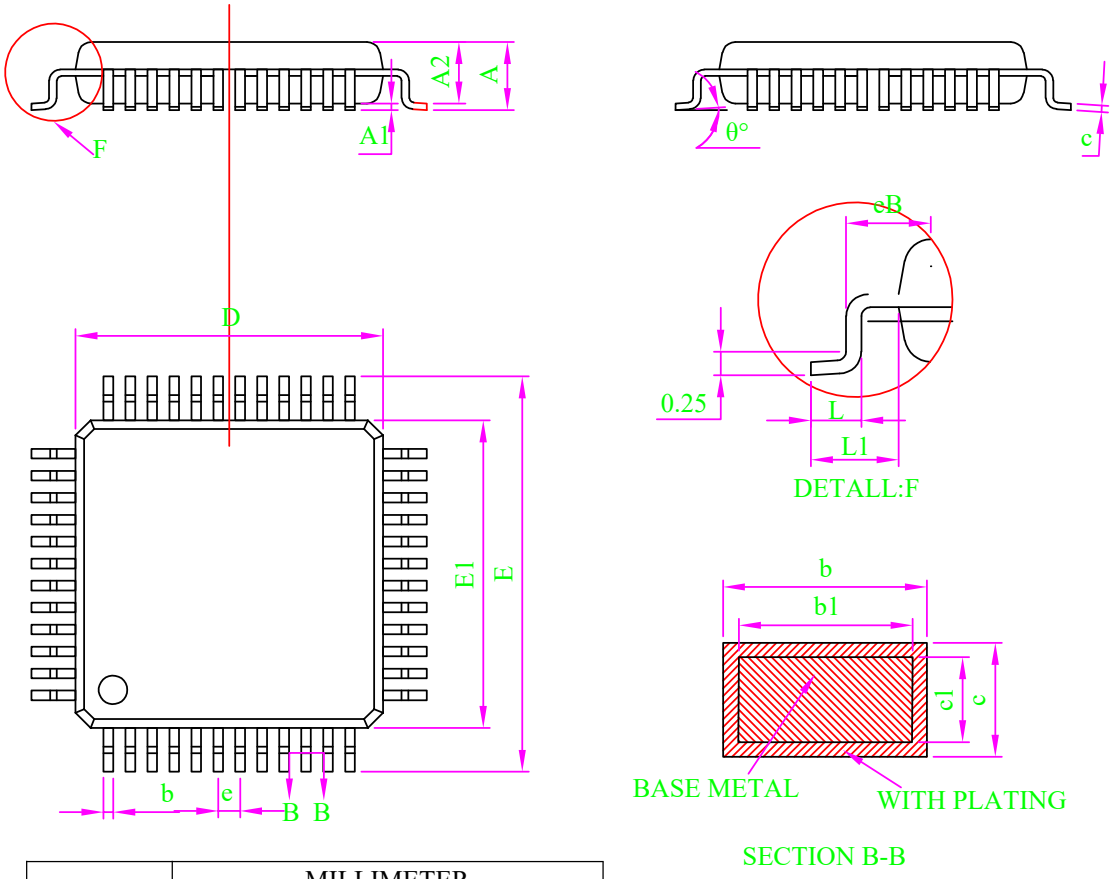
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—		μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tAA
tSU:STA
tSU:STO
S
Sr
P
S

14 Package Information

14.1 LQFP48（7.0mm x 7.0mm PP=0.5mm）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
eB	8.10	-	8.28
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.42	0.57	0.72
L1	0.90	1.00	1.10
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash； Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-19	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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